Effects of Phase Change of Pb-Free Flip-Chip Solders During Board-Level Interconnect Reflow

Soonwan Chung, Zhenming Tang, and Seungbae Park

***Abstract*—The impact of phase change (from solid to liquid) on the reliability of Pb-free flip-chip solders during board-level interconnect reflow is investigated. Most of the current candidates for Pb-free solder are tin-based with similar melting temperatures near 230 °C. Thus, Pb-free flip-chip solders melt again during the subsequent board-level interconnect reflow cycle. Solder volume expands more than 4% during the phase change from solid to liquid. The volumetric expansion of solder in a volume constrained by chip, substrate, and underfill creates serious reliability issues. The issues include underfill fracture and delamination from chip or substrate. Besides decreasing flip-chip interconnect reliability in fatigue, bridging through underfill cracks or delamination between neighboring flip-chip interconnects by the interjected solder leads to failures. In this paper, the volume expansion ratio of tin is experimentally measured, and a Pb-free flip-chip chip-scale package (FC-CSP) is used to observe delamination and solder bridging after solder reflow. It is demonstrated that the presence of molten solder and the interfacial failure of underfill can occur during solder reflow. Accordingly, Pb-free flip-chip packages have an additional reliability issue that has not been a concern for Pb solder packages. To quantify the effect of phase change, a flip-chip chip-scale plastic ball grid array package is modeled for nonlinear finite-element analysis. A unit-cell model is used to quantify the elongation strain of underfill and stresses at the interfaces between underfill and chip or underfill and substrate generated by volume expansion of solder. In addition, the strain energy release rate of interfacial crack between chip and underfill is also calculated.**

***Index Terms*—Contact analysis, flip-chip, interfacial failure, Pb-free solder, phase change, reflow process, strain energy release rate, underfill fracture, volume expansion.**

I. Introduction

LEAD-BASED solders have been used to provide electrical interconnection in electronics packaging for many years. They have merits in cost, wetting characteristics, and availability with various melting temperatures. However, Pb-based solders are to be abandoned due to environmental regulations. The use of Pb-free solders [1], [2] raises concerns that should be addressed in both technical and manufacturing aspects. Compared to Pb-based solders, the technical community does not have the same level of understanding of the behaviors of Pb-free solder candidates, and manufacturing infrastructures are not fully ready to accommodate the new solder systems.

Much research has been conducted in search of Pb-free solder candidates [1]–[5] and, to date, Sn-based solders are accepted generally as the most promising. Most of the reliability data obtained so far is for the ball grid array (BGA), and only a few studies have been reported for Pb-free flip-chip interconnects. There are very few reports related to solder joint reliability when Pb-free solders are used in both flip-chip and board-level interconnects. The solder in Pb-free flip-chip interconnects melt during the board-level reflow since most Pb-free solders (e.g., Sn–Ag, Sn–Cu, Sn–Ag–Cu) have similar melting temperatures in the range 220 °C–240 °C [3] while board-level reflow temperature is 250 °C–260 °C. Pb-free solder expands in volume due to the phase change from solid to liquid, and this exerts a high hydrostatic pressure on the surrounding boundaries defined by underfill encapsulation. This pressure stretches the underfill and generates significant stress in the underfill/die or underfill/substrate interfaces. The coefficient of thermal expansion (CTE) of the underfill above glass transition temperature is typically in the order of hundreds of ppm/°C which is several orders of magnitude smaller than the volume expansion of the solder. Depending on the maximum elongation strain of the underfill and maximum strength of the interfaces, underfill cracking or delamination may occur. It generates a concern about bridging of the adjacent flip-chip solders by the flow of solder through the delamination or crack during the board-level reflow, currently, there is no reliability check item in place for such a concern. Fig. 1 illustrates the mechanism. Genovese *et al.* [6] have reported failures caused by solder extrusion at the interfaces of either the die passivation/underfill or solder mask/underfill after multiple board-level reflows.

In this study, the volume expansion of Pb-free solder during solid to liquid phase change is quantified. Subsequently, the effect of such a volume change of the flip-chip solder is investigated experimentally. A quantitative assessment is performed numerically using finite-element analysis (FEA). A flip-chip chip-scale package (FC-CSP) is used for this work. To help visualization, Pb-free board-level interconnect solders (BGAs) are underfilled and subjected to a simulated board-level reflow cycle. The X-ray and the cross-section images taken before and after the reflow clearly indicate the delamination and short circuit due to the solder extruded through the failure.

II. Experiments

A. Solder Volume Expansion During Phase Change

The volume expansion ratio of Pb-free solder during phase change was measured experimentally. Since the major component of Pb-free solder is tin, i.e., 95%+ tin, the expansion of pure tin was measured in this study. Fig. 2 shows the experimental setup which is composed of a glass tube and thermal chamber.

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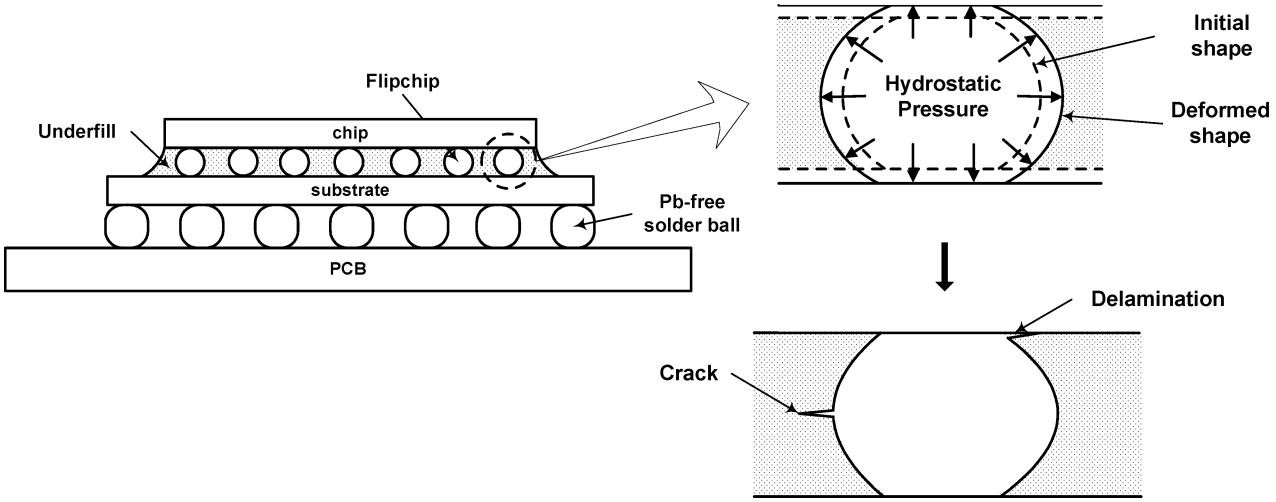

Fig. 1. Schematic of underfill delamination and crack during board-level reflow.

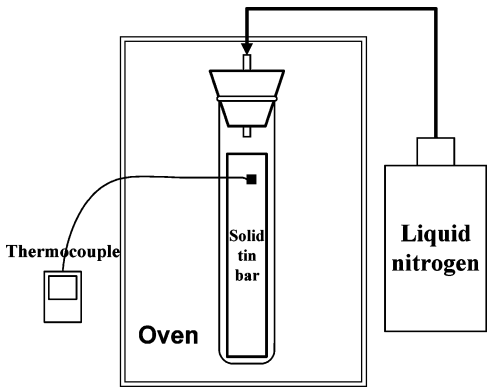

Fig. 2. Schematic of experimental setup for volume expansion measurement.

The solid tin bar of 12.7-mm diameter was washed by HCl acid and then rinsed by distilled water to remove surface oxides built up on the tin bar. The tin bar was X-rayed to check possible void entrapment. Then, the mass and the volume of the tin bar were measured. The solid tin bar was put in the test tube and an inert gas, nitrogen, was filled in the test tube to prevent the generation of tin oxide during heating. It is important to minimize the generation of tin oxide since the tin oxide does not melt at the melting temperature of the bulk tin. Although the melting temperature of the tin is 232 °C, it was heated up to 260 °C to ensure that all the tin would melt. When the solid tin was completely molten after 30 min in 260 °C, the volume of liquid tin was recorded. Finally, the liquid tin was solidified, and its mass was measured again to confirm that mass was conserved. Two different lengths of tin bar were used in this experiment. Table I shows the results for the two solid tin bars. The average volume expansion ratio is 4.32%.

The volume expansion during phase change from solid to liquid can be calculated by using the density difference in solid and liquid phase as shown as follows:

$$\beta = \frac{V_l - V_s}{V_s} = \frac{V_l}{V_s} - 1 = \frac{\rho_s}{\rho_l} - 1 \qquad (1)$$

TABLE I
DATA FOR VOLUME EXPANSION EXPERIMENT

	Volume of solid tin (ml)	Volume of liquid tin (ml)	Volume expansion rate (%)
Test 1	12.90	13.43	4.11
Test 2	18.09	18.91	4.53

where V_s and V_l are the volumes of tin in the solid and liquid states, respectively, and ρ_s and ρ_l are the densities as solid and liquid, respectively. From the published densities of pure tin in solid and liquid state,[1] the volume expansion ratio is calculated as follows:

$$\beta = \frac{\rho_s}{\rho_l} - 1 = \frac{7288.4(\mathrm{kg/m^3})}{7000.1(\mathrm{kg/m^3})} - 1 = 4.1(\%). \qquad (2)$$

It validates the current test result in the order of 4% volume expansion during the phase change.

B. Underfill Delamination During Board-Level Reflow

Pb-free FC-CSPs were thermal cycle tested to observe the delamination at the interface or crack in the underfill after a simulated board-level reflow. Fig. 3(a) shows a side view of the sample used. To visualize such a failure more clearly, board-level BGA SAC (Sn–Ag–Cu) solder balls in an 8 × 8 array were underfilled as shown in Fig. 3(b). The pitch of BGA is 0.8 mm, the maximum diameter of solder balls is 0.5 mm, and the sizes of chip and substrate are 6.5 mm by 6.5 mm and 10 mm by 10 mm, respectively. Two different kinds of underfill, UF-A and UF-B, were used. The material properties of two underfills are presented in Table II. UF-A features low CTE and improved toughness, so this material is specially suited for flip-chip devices requiring crack/fracture resistance. UF-B exhibits low moisture absorption for improved Joint Electron Device Engineering Council (JEDEC) performance. The package went through a typical Pb-free BGA reflow cycle with the peak temperature 250 °C and then was cooled to room temperature.

[1][Online]. Available: http://www.daltonelectric.com/engineering-data-and-design-considerations.htm

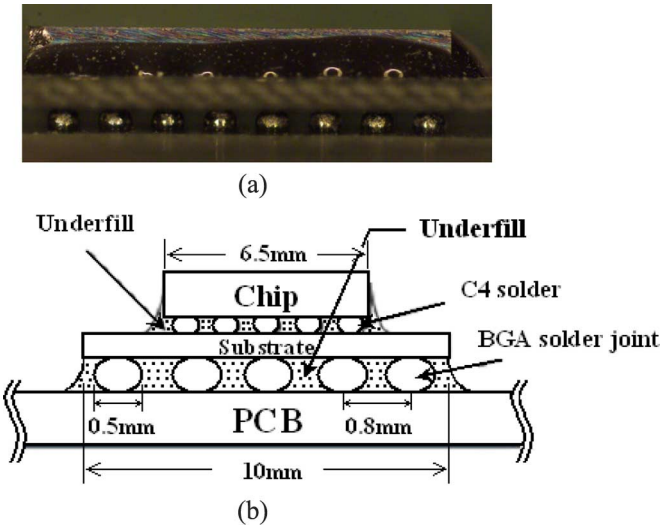

Fig. 3. FC-CSP used for solder reflow test. (a) Side view of thermal cycle test specimen before underfilling BGA. (b) Schematic after underfilling BGA.

TABLE II
MATERIAL PROPERTIES OF UNDERFILL FOR ENCAPSULATION OF FLIP-CHIP DEVICES

	Glass transition (T_g) (℃)	CTE (ppm/℃)	Flexural modulus (GPa)	Filler content (%)
UF-A	120	22 (below T_g) 84 (above T_g)	9.5	64
UF-B	140	45 (below T_g) 143 (above T_g)	5.6	50

To inspect the solder extrusion during phase change, X-ray images before and after reflow are compared and the cross-sectional analyses of the packages are performed. Fig. 4 shows X-ray images. It is revealed that the formation of molten solder is followed by bridging between two solder balls and the sizes of many solder balls are changed (or reduced) as shown in Figs. 4(b) and (c). Specifically, the solder is seen between E03 and E04 solder balls with UF-A and between F05 and F06 solder balls with UF-B. The hydrostatic pressure due to solder volume expansion exceeded the interfacial bonding strength or caused a crack to initiate and/or propagate, and pushed the molten solder into the adjacent voids.

To further investigate the delamination and determine the shape of void, cross-sectional analyses are performed. The packages are ground from the right side (column H) toward column A. The cross section of two packages with different underfill materials are shown in Figs. 5 and 6. It is clear that part of E03 solder has moved to the adjacent void as shown in Fig. 5(a). However, it is not clear whether it was pre-existing or newly created. In the meantime, the volume of E03 solder is decreased as the same amount as the adjacent empty volume as seen in Fig. 5(b). Also, the generation of the void in Fig. 5(c) and the delamination between underfill and substrate in Fig. 5(d) are observed. Naturally, more detailed information on the failure around the interfaces is revealed from the cross-sectional analysis. Similar results are observed in a sample with UF-B underfill as shown in Fig. 6. In this case, the delamination occurred between underfill and substrate at F06

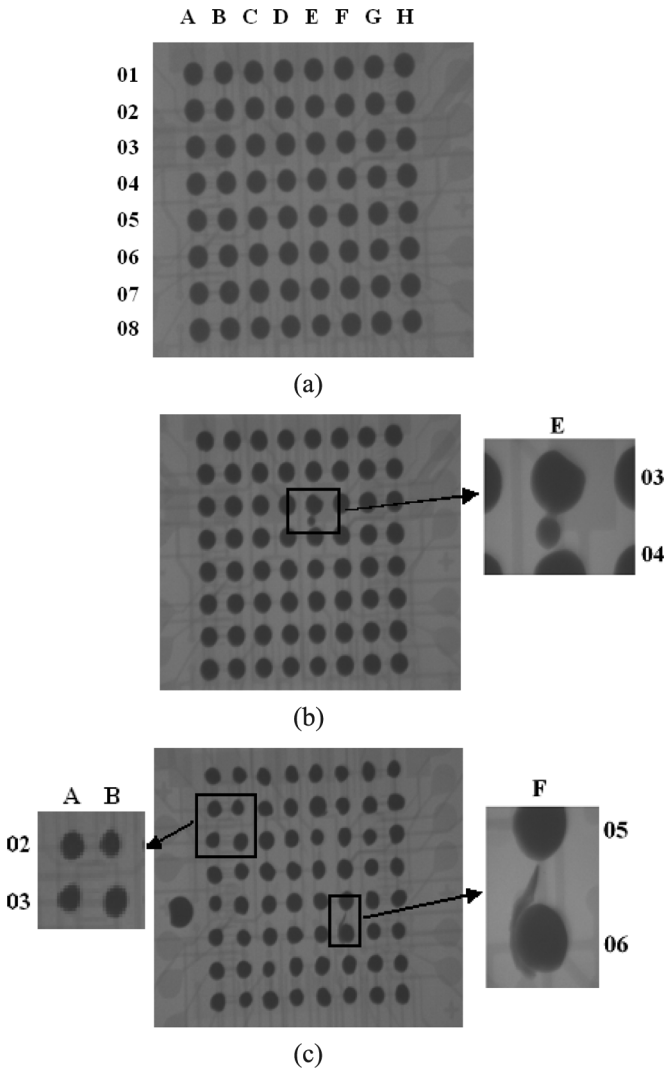

Fig. 4. X-ray images of underfilled BGA of FC-CSP (top view). (a) Before reflow process. (b) After reflow process (UF-A). (c) After reflow process (UF-B).

solder ball Fig. 6(a) and the solder bridging shown in Fig. 4(c) have occurred through the gap of the delamination. Bigger voids and larger delamination are presented in Fig. 6(b) and (c). These experimental results confirm that the reflow of Pb-free solder generates delamination and solder bridging of the flip-chip interconnects during board-level reflow.

III. NUMERICAL SIMULATION OF PHASE CHANGE

The underfill around flip-chip solder is expected to undergo significant total strain with more than 4% volumetric expansion. Fig. 7 illustrates the deformation of the underfill during the phase change of the solder. The molten solder acts as a hydraulic fluid pushing the chip and substrate primarily in the vertical direction because the underfill side walls (shown as vertical centerlines in Fig. 7) have the same amount of pressure transmitted from the neighboring solders. The resultant strain at the surrounding underfill is investigated quantitatively. Also, it is not unusual to observe formation of voids and/or a weak interface between the underfill and die or the underfill and substrate due to flux residue after the underfilling process. These act as pre-existing cracks in the package. Therefore, the model with a

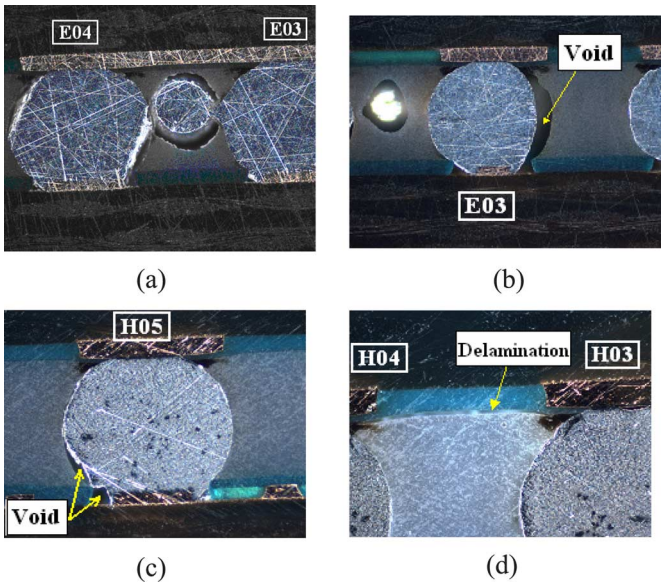

Fig. 5. Cross-sectional images of FC-CSP with UF-A. (a) E04 and E03 solder balls at a cross section. (b) E03 solder ball at deeper section. (c) H05 solder ball. (d) Between H04 and H03 solder balls.

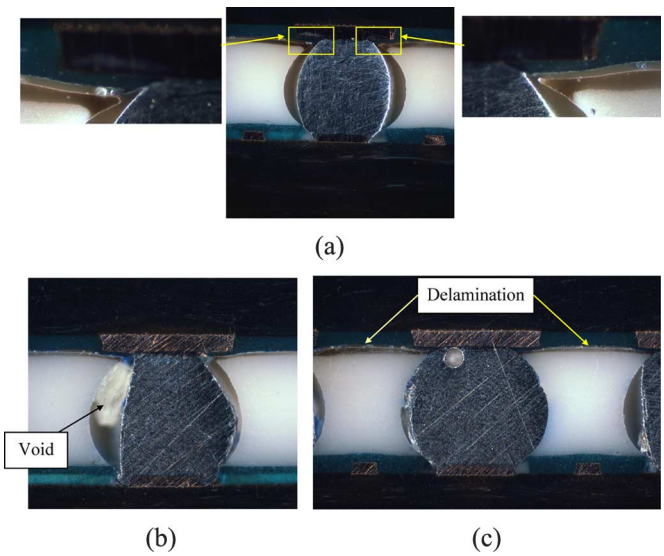

Fig. 6. Cross-sectional images of FC-CSP with UF-B. (a) F06 solder ball. (b) H01 solder ball. (c) H03 solder ball.

pre-existing crack is also analyzed to investigate whether or not the volume expansion of solder propagates the crack.

A. FEA Models

A unit-cell configuration of a flip-chip is considered with a coupled boundary condition, which is the constraint condition to make all the nodes assigned to move together. This condition is applied to the right side of the computational domain by deliberating the force equilibrium at the underfill side wall due to the pressure transmitted from the neighboring solders as shown in Fig. 7. The flip-chip solder dimensions used are 100-μm diameter at top/bottom pad and 140-μm diameter at the maximum bulge. The model assumes an axisymmetric condition as shown in Fig. 8. The Pb-free solder material is modeled as pure tin. The

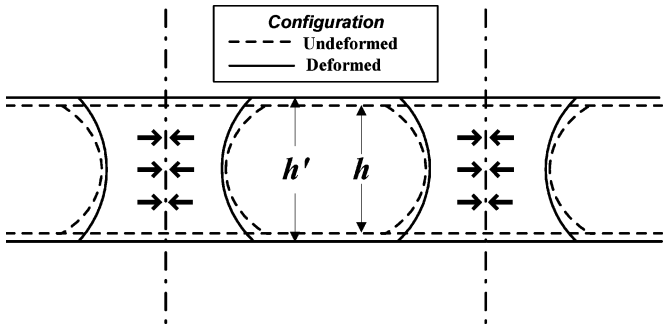

Fig. 7. Schematic of deformed underfill.

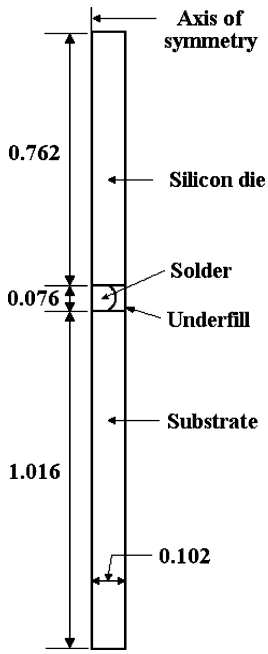

Fig. 8. Schematic of axisymmetric model for analysis (unit: millimeters).

phase change of Pb-free solder is simulated by using fluid element for the solder. The equivalent value of CTE to the volume expansion during phase change was calculated and applied to the arbitrarily chosen temperature change 3 °C (from 232 °C to 235 °C). It is because the thermal deformation of the materials other than solder should be minimal during the temperature change. The mechanical properties of each material are shown in Table III. The Young's modulus for the solder that is shown is the bulk modulus of liquid tin. In this study, the Young's modulus and CTE of the underfill correspond to those shown for the case above the glass transition temperature (T_g). Linear fluid elements (FLUID79) are used for modeling the solder, and other materials are modeled by quadratic (eight-node for quadrilateral and six-node for triangular) solid elements (PLANE82). The contact boundary condition is assigned at the interface between liquid solder and neighboring materials where the outline of solder is chosen as contact surface (CONTA172) and the corresponding lines of other materials are chosen as target surfaces (TARGE169). For the case of a pre-existing crack, a crack is introduced at the interface between silicon die and underfill in a length of 12.7 μm. Fig. 9 shows the finite-element mesh. The

TABLE III
MECHANICAL PROPERTIES OF MATERIALS USED

	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/℃)
Silicon die	162	0.28	3
Ceramic substrate	299.9	0.23	8
Underfill (UF-C)	5.49 (below T_g) 0.05 (above T_g)	0.33	26 (below T_g) 88 (above T_g)
Solder (pure tin)	58 (Bulk modulus)	-	4556 (232~235 ℃)

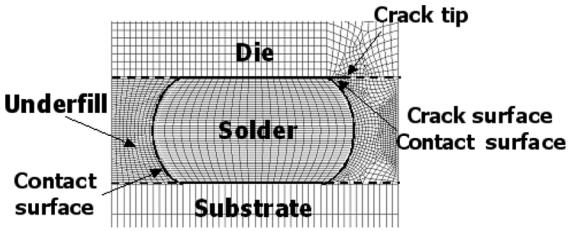

Fig. 9. Finite-element mesh of interfacial crack model.

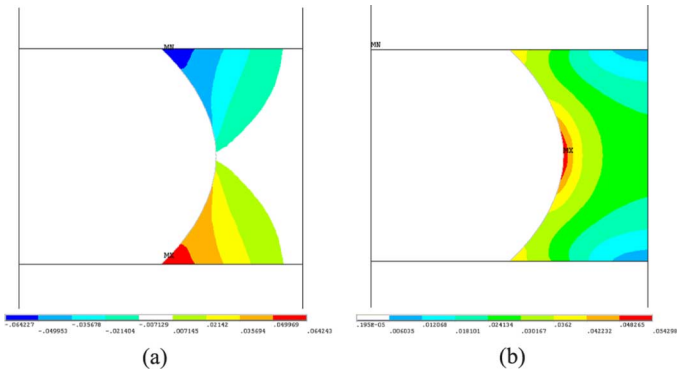

Fig. 10. Strain distributions of axisymmetric model. (a) Shear strain (ε_{xy}). (b) Von-Mises strain (ε_{vm}).

commercial finite-element program ANSYS 9.0[2] is utilized for numerical analyses. The plane strain condition is assumed.

B. FEA Results

The strains resulting from using the axisymmetric unit-cell model are shown in Fig. 10. The actual height increase of solder and underfill in Fig. 7 ($\Delta h = h' - h$) is about 2%. Since the Young's modulus of the underfill is much lower than that of the die or substrate, most strain occurs at the underfill. The underfill around the solder bulge has the maximum von-Mises strain as much as 5.4% as shown in Fig. 10(b). The maximum strain seems to be serious in view of the ultimate strain 1.39% at room temperature .

Fig. 11 shows that the von-Mises stress of the interfacial crack is concentrated around the crack tip. By using the modified crack closure method [7]–[9], the strain energy release rate is calculated to judge whether the crack will propagate or not. The

[2]ANSYS University Advanced, Release 9.0.

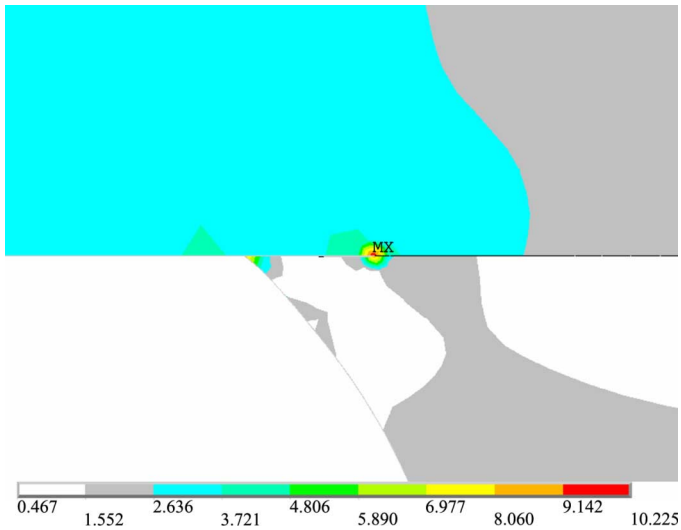

Fig. 11. Von-Mises stress distribution around crack tip of interfacial crack model (unit: megapascals).

strain energy release rates for mode-I and mode-II are $G_I = 0.0563$ (J/m^2) and $G_{II} = 0.1673$ (J/m^2), respectively, and the total strain energy release rate (G_T) is 0.2236 (J/m^2). It means that in-plane shear is more dominant than in-plane tension during volume expansion of solder. When the interfacial fracture toughness of a underfill at its mating interface such as die passivation or substrate is lower than this strain energy release rate, the crack propagates and the solder is extruded through the created crack.

At this stage, it is required to estimate the level of severity of the calculated strain energy release rate as a crack driving force. Since the critical strain energy release rate below T_g of the underfill is available in the literature, the strain energy release rate during the phase change is recalculated using Young's modulus below T_g of underfill. The calculated G_T, 31.53 (J/m^2) is within the range of published critical strain energy release rate of passivated silicon Si_3N_4/Si, i.e., between 14.0 and 68.5 J/m^2 [10], [11]. Therefore, depending on the initial crack length, the interface between passivated silicon (Si_3N_4/Si) and the underfill may be at the risk of delamination due to the phase change of the solder.

IV. CONCLUSION

In this paper, the reliability impact of the phase change of Pb-free solder on flip-chip package is investigated experimentally and numerically. Due to the deficiency of soldering hierarchy between chip-level and board-level interconnects of Pb-free flip-chip package, it raises reliability and manufacturing yield concerns which do not exist in conventional Pb-based solder packages. The following conclusions are made.

1) Pb-free solder shows 4%+ volume expansion during phase change from solid to liquid.
2) From the board-level interconnect reflow process, the underfill failure and bridging by solder extrusion are observed.
3) During simulated board-level reflow, the underfill is subjected to a high elongation strain. The underfill cracking

is expected by numerical analysis and actually observed in controlled experiment.

4) The calculated strain energy release rate is in the range of interfacial fracture toughness of an interface between underfill and passivation layer of the silicon. This result is supported by the solder extrusion at the interface in the controlled experiment.

Adhesion promotion between underfill/die or underfill/substrate is recommended for Pb-free flip-chip packages. Additional reliability checks on packages, especially for bridging in the chip-level interconnect after the board-level interconnect reflow is highly recommended.

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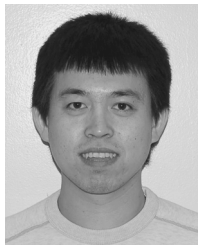

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