Shorter Field Life in Power Cycling for Organic Packages

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The importance of power cycling as a mean of reliability assessment was revisited for flip chip plastic ball grid array (FC-PBGA) packages. Conventionally, reliability was addressed empirically through accelerated thermal cycling (ATC) because of its simplicity and conservative nature of life prediction. It was well accepted and served its role effectively for ceramic packages. In reality, an assembly is subjected to a power cycling, i.e., nonuniform temperature distribution with a chip as the only heat source and other components as heat dissipaters. This non-uniform temperature distribution and different coefficient of thermal expansion (CTE) of each component make the package deform differently than the case of uniform temperature in ATC. Higher substrate CTE in a plastic package generates double curvature in the package deformation and transfers higher stresses to the solder interconnects at the end of die. This mechanism makes the solder interconnects near the end of die edge fail earlier than those of the highest distance to neutral point. This phenomenon makes the interconnect fail earlier in power cycling than ATC. Apparently, we do not see this effect (the die shadow effect) in ceramic packages. In this work, a proper power cycling analysis procedure was proposed and conducted to predict solder fatigue life. An effort was made for FC-PBGA to show the possibility of shorter fatigue life in power cycling than the one of ATC. The procedure involves computational fluid dynamics (CFD) and finite element analyses (FEA). CFD analysis was used to extract transient heat transfer coefficients while subsequent FEA–thermal and FEA–structural analyses were used to calculate temperature distribution and strain energy density, respectively. [DOI: 10.1115/1.2429706]

Keywords: power cycling, FEA, CFD, flip chip PBGA, ATC, ANSYS, ICEPAK

Introduction

Fatigue failure of solder interconnect is a major reliability concern in electronics packaging. Temperature fluctuations caused by either power consumption or environmental changes, along with the resulting thermal expansion mismatch between the various package materials result in deformation stresses in packages/assemblies especially in solder interconnects. Accelerated thermal cycling (ATC) have long been performed to assess reliability of solder interconnects where the entire assembly is subjected to uniform temperature change in an environment chamber (heating/cooling), meanwhile, actual package (or assembly) is experiencing nonuniform temperature distribution in the assembly having the chip as the source of heat generation. Consequently, it is obvious that ATC does not truly represent real service conditions.

There is another way of reliability testing called power cycling (PC). To mimic the reality, only the chip is powered while other components are acting as heat dissipaters. Traditionally, ATC is conceived to generate harsher environment than PC. In other words, ATC is predicting its life conservatively. It is generally true for ceramic packages. Ceramic substrate has higher flexural rigidity and the second level interconnect failure is mostly due to the shear deformation driven by thermal expansion mismatches between substrate and printed circuit board (PCB). Ceramic packages have been used for high-end and/or higher reliability applications partially due to the higher level of understanding of its service life. Testing its life with ATC made the reliability projection more conservative and accordingly ATC was accepted as standard test method. The average shear strain (γ) of the solder ball at maximum distance to neutral point (DNP) is described in Eq. (1), also refer Fig. 1.

$$\gamma = \frac{L}{2h}(\alpha_{PCB}\Delta T_{PCB} - \alpha_{SUB}\Delta T_{SUB}) \tag{1}$$

In ATC, due to the uniform temperature, $\Delta T_{PCB} = \Delta T_{SUB} = \Delta T$. Hence, for ATC the shear strain (γ_{ATC}) can be expressed as

$$\gamma_{ATC} = \frac{L}{2h}(\alpha_{PCB} - \alpha_{SUB})\Delta T \tag{2}$$

Shear strain (γ) depends on the CTE difference between the substrate and the PCB. In case of PC, as the chip is the source of heat generation and other components such as substrate and PCB act as heat spreaders, it is natural to have $\Delta T_{PCB} < T_{SUB}$ and thus Eq. (3) cannot be simplified as Eq. (2)

$$\gamma_{PC} = \frac{L}{2h}(\alpha_{PCB}\Delta T_{PCB} - \alpha_{SUB}\Delta T_{SUB}) \tag{3}$$

For typical Ceramic packaging, since $\alpha_{PCB} > \alpha_{SUB}$ and $\Delta T_{PCB} < \Delta T_{SUB}$, it is always true that $\gamma_{ATC} > \gamma_{PC}$. However, in case of organic packages, there are possibilities of $\gamma_{ATC} < \gamma_{PC}$ depending upon CTE, ΔT_{PCB} and ΔT_{SUB}. Therefore, PC may generate severe condition than ATC and the assembly that passed life test with ATC may not be safe in the field within its service life. In this regard, detailed analysis of power cycling is required for the organic (or plastic) packaging. Power cycling simulation is a flow-thermo-mechanical analysis wherein integration of the interrelated quantities such as transient heat transfer coefficients, temperature, and deformation in and around the assembly in a convective environment is required [1].

In previous studies of power cycling simulation, use of integrated thermo-mechanical analysis methods was recommended for solder joint reliability of various ball grid array packages. Darveaux and Mawer presented a comprehensive study on thermal and power cycling limits of a wire bond based 225-ball plastic ball grid array (PBGA) assembly with Sn62–Pb6–2Ag solder joints at a pitch of 1.5 mm [2,3]. Hong et al. performed integrated

Contributed by the Electrical and Electronic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received March 23, 2005; final manuscript received May 1, 2006. Review conducted by Dereje Agonafer. Paper presented at the ITHERM 2004.

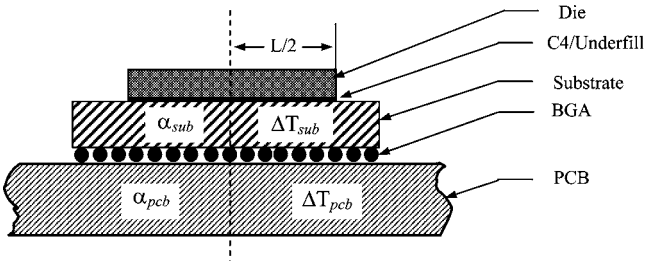

Fig. 1 Typical FC-PBGA package

flow-thermo mechanical and reliability analysis of a flip chip PBGA package under power cycling conditions [1]. Subarrayan et al. conducted work to correlate accelerated thermal cycling and power cycling [4]. Rodgers et al. made efforts in comparison between ATC and PC, and showed that PC was more benign condition [5]. In this study, integration of transient heat-transfer coefficients using a computational fluid dynamic (CFD) tool and thermal/structural finite element analysis (FEA) was conducted to show the impact of power cycling in organic packaging (see Fig. 1).

Package Specification

The package used in this study is a flip chip plastic ball grid array (FC-PBGA) assembly. Figure 2 shows cross-sectional and top views of the assembly. The package has 7×17 eutectic (62Sn–36Pb–2Ag) solder balls with a pitch of 1.27 mm and is assembled to a $76\times76\times1.57$ mm FR4 printed circuit board. The chip size is $10\times14\times0.75$ mm and joined to a BT (bismaleimide triazine) substrate in the size of $22\times14\times0.7$ mm by Flip Chip C4 interconnects. The C4 is underfilled for the protection. Material properties of the assembly are listed in the Tables 1–3 [1].

Table 1 Thermal properties

Material	Density (lb./in.^{3})	Sp.heat (J/lb. K)	Conductivity (J/s/in. K)
Silicon	0.08417	322.94	2.7939
C4/underfill	0.21965	305.71	0.0406
Copper	0.32305	174.622	9.88
BT-laminate	0.07207	539.76	0.07619
Pb37–Sn63 solder ball	0.23374	68.025	1.29539

Procedure

The first step in the projection of component reliability through power cycling was modeling of the assembly using CFD to extract transient heat transfer coefficients under the assumption that surrounding air is at room temperature with laminar flow around the package. CFD was performed using commercial ICEPAK software [6]. It should be noted that CFD model has much coarse mesh than FEA model. However, ICEPAK provides transient heat transfer coefficient across each coordinate of the model surface. Then those values are averaged in each area of the following FEA models to maintain the total heat flux. The second step is FEA—thermal analysis using commercial ANSYS software [7]. The thermal element, SOLID70, was used and transient heat transfer coefficients obtained from CFD were applied as boundary conditions

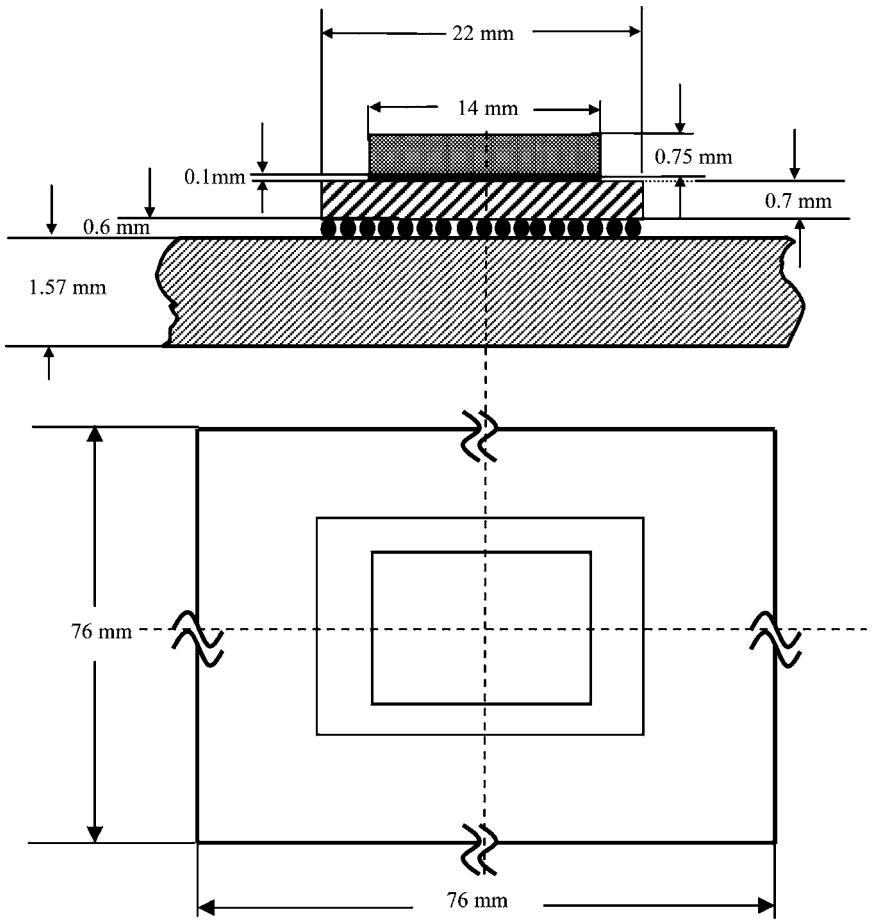

Fig. 2 119 (7×7) BGA I/O FC-PBGA—front view and top view

Table 2 Mechanical properties

Material	Temp (K)	Modulus (psi)	Poisson ratio	CTE (ppm/C)
Silicon	—	2.35×10^7	0.28	3
C4/underfill	—	2.09×10^6	0.28	20
Copper	—	9.99×10^6	0.34	17
BT-laminate	—	3.77×10^6	0.39	17
	—	1.59×10^6	0.11	52
PCB (FR4) $-x$, z, y	—	3.19×10^6	0.28	17
	—	1.45×10^6	0.11	70
Pb37–Sn63	265	3.83×10^6	0.360	25.2
solder ball	323	1.81×10^6	0.365	26.1
	380	1×10^6	0.378	27.3

on the areas of die, substrate, and PCB. Also, power generation was applied to the chip. Third step is FEA—structural analysis using structural elements SOLID45/VISCO107, with transient nodal temperatures imported from the FEA thermal analysis as loading conditions. Finally, in the fourth step, modified strain energy based approach is adopted in projection of relative reliability of the assembly. Figure 3 outlines the approach of the proposed power cycling analysis.

Computational Fluid Dynamics (CFD)

Complete assembly was modeled with 119 BGA and subjected to cyclic power of 3 W. The chip was powered for 800 s with the cyclic period of 1600 s. Figure 4 shows the schematic of the cycle. A cabinet in the CFD model was created to have a domain size of 4.5 in. in length (x direction), 4.5 in. in width (y direction), and 3.14 in. in height (z direction). Computational domain in Cartesian coordinates is shown in Fig. 5. A fan was modeled with

Table 3 Constants for solder constitutive equations

ANSYS	Parameter	Values
$C1$	S_0(psi)	1800
$C2$	Q/k(1/K)	9400
$C3$	A(1/s)	4.0E6
$C4$	ε	*1.5*
$C5$	m	0.303
$C6$	h_0(psi)	2.0E5
$C7$	S^(psi)	2.0E3
$C8$	n	0.07
$C9$	a	1.3

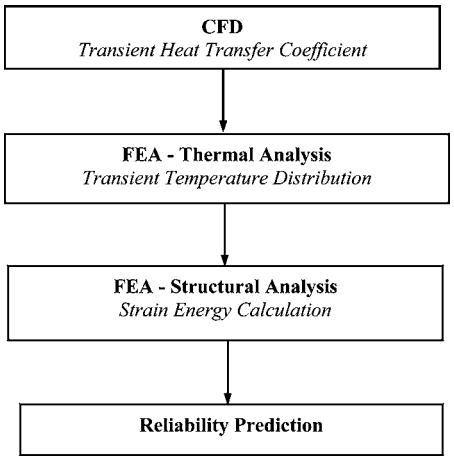

Fig. 3 Schematic outline to predict solder life through power cycling

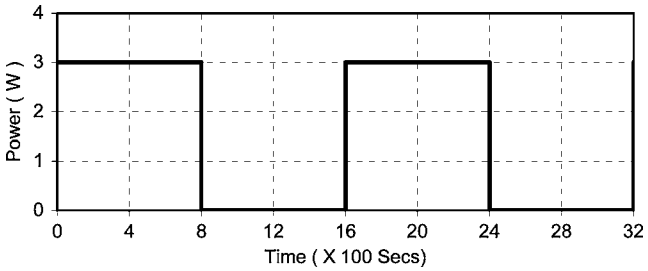

Fig. 4 Chip power cycle load

airflow velocity of 0.33 ft/s on the y-z plane with laminar flow. A vent is modeled with dimensions equivalent to the face of the cabinet. Mesh sensitivity study showed that 32,342 elements are appropriate for solution convergence. Modeled assembly was power cycled and the surrounding ambient temperature of 25°C was initialized. Variables in CFD were flow (velocity/pressure) and temperature. Inlet conditions are set with uniform initial velocity and temperature distributions. Adiabatic thermal conditions are assumed at the top, bottom, and sidewall of the cabinet. Gravity effect was included in this forced convection heat transfer analysis. Number of iterations per time step was 20 with convergence flow and energy criteria as 0.001 and 1e-6, respectively. Assuming incompressible laminar and steady flow, the governing conservation equations with appropriate boundary conditions were solved. After running the simulation, local transient heat transfer coefficients and temperature distributions were obtained. The transient heat transfer coefficients from surfaces were stored as text files and they were applied as boundary conditions in FEA-thermal analysis. Critical to the integration of CFD and FEA-thermal analysis was efficient extraction and application of heat transfer coefficients using macro language in ANSYS. Figure 6 shows temperature profile of the chip powered at 800 s.

FEA—Thermal Analysis

A three-dimensional quarter symmetry model was created for sequential transient heat transfer and nonlinear stress analyses (see Fig. 7). Since direct coupling of thermal and structural analysis incorporating visco-plastic elements is currently not available in commercial FEA package, the analysis was divided into thermal and structural analysis. Eight-Noded 3D Solid element, Solid 70, was used for FEA—thermal analysis. The predetermined thermal boundary condition of local heat transfer coefficients was applied on all the surface areas in the transient thermal finite element model. Cyclic chip power load of 3 W was applied to calculate transient nodal temperature for the entire assembly. Temperatures obtained from transient thermal analysis are saved as loading conditions for the subsequent FEA-structural analysis.

Figures 8 and 9 show temperature profile in the cross section and the top surface of the assembly. It should be noted that contour profile is taken at the end of first load cycle, i.e., at 800 s. The temperature gradient through the thickness of the package is apparent in the chip area. As shown in Fig. 9, temperature profile is not symmetric about the vertical axis due to the difference in heat transfer coefficients across the leading and trailing edge of the assembly in the airflow. In this analysis, the trailing section is modeled as the quarter symmetry since temperature gradient is higher and thus generates a worse condition for solder interconnects.

The temperature profiles were compared for CFD and FEA-thermal analyses at several points and it can be observed that temperature profiles calculated by FEA match fairly well those of CFD (Fig. 10). The minor discrepancies stemmed out of the artificial quarter symmetry model in FEA-thermal to reduce the com-

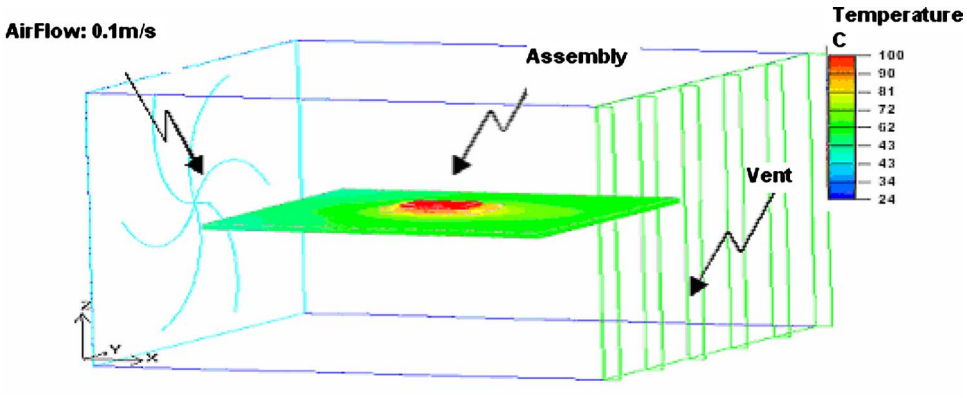

Fig. 5 Complete assembly in ICEPAK

putational budget. The analysis reveals that the power cycling generates severe variation in both in-plane and out-of-plane temperatures.

FEA—Structural Analysis

An eight-noded three-dimensional (3D) solid thermal element in FEA-thermal analysis was replaced by an eight-noded SOLID 45/VISCO107 element for structural analysis. It should be noted that for sequential thermal/structural analysis, selection of element is key to assuring compatibility and solving convergence problems. Eight-noded elements, therefore, were used throughout the analysis. Symmetry boundary conditions were imposed and the central node of the package was fully restrained to prevent rigid body motion. Figures 11 and 12 show warpage distribution in power cycling and ATC at the midplane of die, substrate and PCB in their maximum deformation. In the case of power cycling, three cycles of transient nodal temperatures obtained from FEA–thermal analysis were applied with starting temperature and stress free conditions at 100°C. Accelerated thermal cycling was also performed for comparison. For ATC, three cycles of (25–100°C, 480 s ramps/320 s dwells) were applied throughout the assembly. In Fig. 12, we observe that the substrate warps until the die ends and then it relaxes, producing a wave-like deformation mechanism, i.e., double curvature. This double curvature causes the solder interconnects to experience more stress, thus accelerating the failure in organic packages [3].

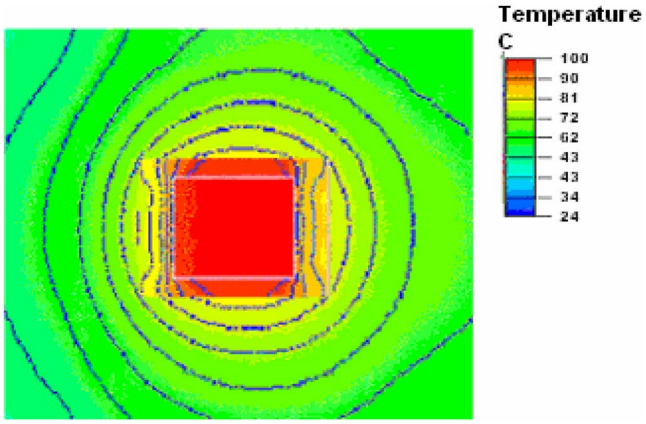

Fig. 6 Temperature contour profile of simulated package using CFD

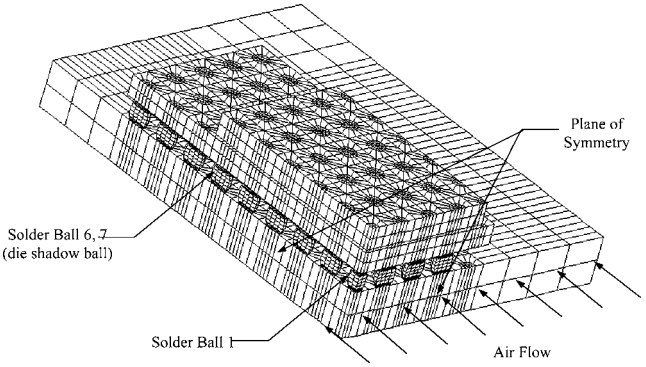

Fig. 7 Quarter symmetry model of flip chip PBGA package in ANSYS

Component Reliability Prediction

In Darveaux's energy method [8], to predict characteristic fatigue life of each solder joint, accumulated plastic work per cycle

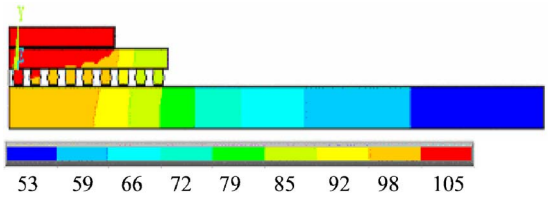

Fig. 8 Temperature profile in the cross section of the assembly

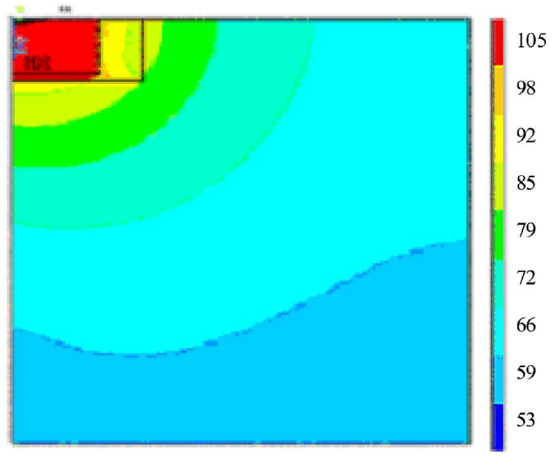

Fig. 9 Temperature profile at the top surface of the assembly

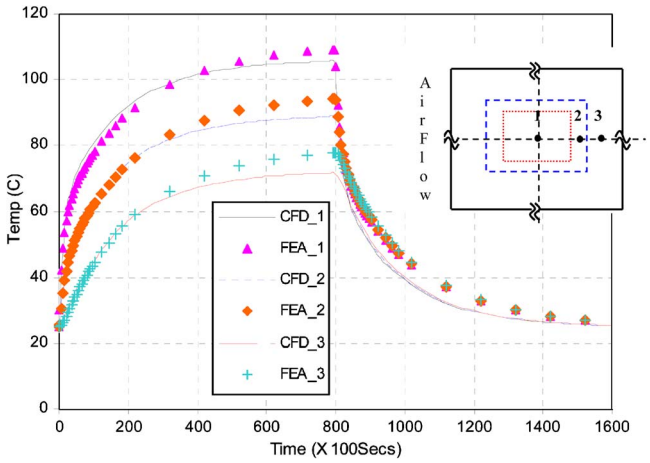

Fig. 10 Temperature profile of reference points

is averaged across the elements along the solder joint interface where the crack propagates. The equation for stabilized change in average plastic work (ΔW_{ave}) is given in Eq. (4)

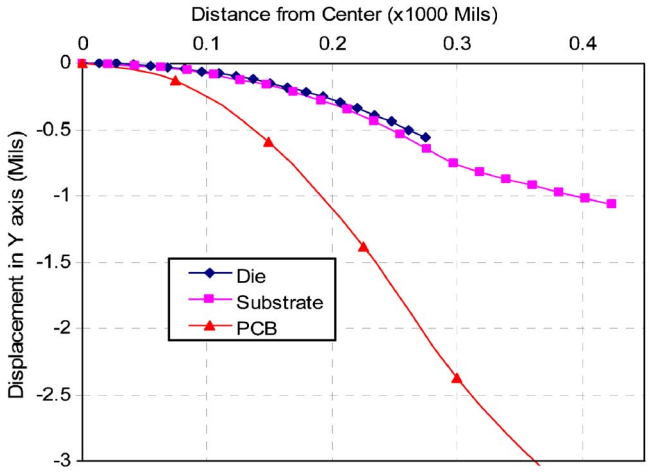

Fig. 11 Warpage distribution at the midplane of chip, substrate, and PCB for power cycling

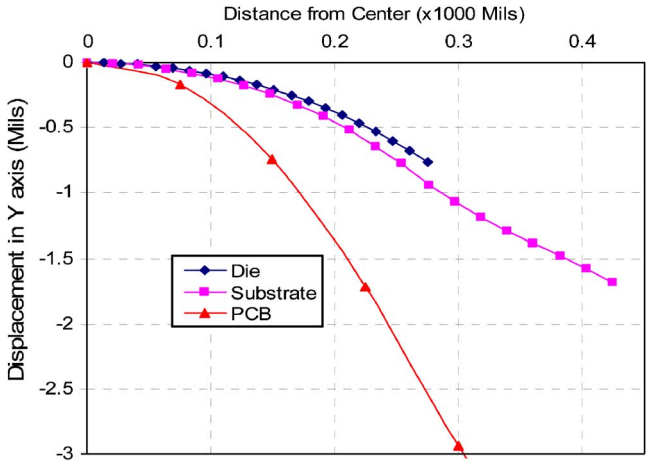

Fig. 12 Warpage distribution at the midplane of chip, substrate, and PCB for ATC

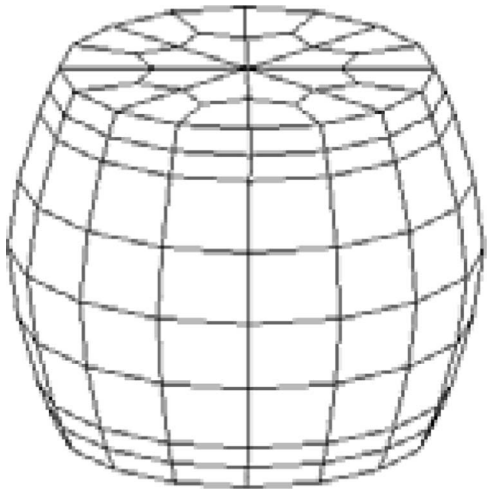

Fig. 13 Two layers of 1.0 mil thickness on the top and bottom surface of the solder joint

$$\Delta W_{ave} = \frac{\Sigma(\Delta W \bullet V)}{\Sigma V} \tag{4}$$

Calculation of thermal cycles to crack initiation and crack propagation rate per thermal cycle are given by Eqs. (5) and (6)

$$N_o = K1(\Delta W_{ave})^{K2} \tag{5}$$

$$\frac{da}{dN} = K3(\Delta W_{ave})^{K4} \tag{6}$$

Characteristic solder joint fatigue life can then be calculated by summing the cycles to crack initiation with the number of cycles taken by crack to propagate across the entire solder joint diameter shown in Eq. (7)

$$\alpha = N_o + \frac{a}{da/dN} \tag{7}$$

Solder joint model constructed has finer mesh, it is provided with two layers of 1.0 mil thickness near the top and bottom surface as shown in Fig. 13.

To evaluate characteristic life, ΔW_{ave}, i.e., element volumetric average of the stabilized change in plastic work within the controlled eutectic solder element thickness was used. Darveaux suggested the crack growth constants ($K_1 - K_4$) for 1.0 mil as listed in the Table 4. But, in this work, maximum accumulated plastic work per cycle was used in place of ΔW_{ave}. This approach was used to achieve more realistic crack initiation across the solder interconnects since averaging of plastic work has a tendency to overpredict the life of solder interconnects.

Results and Discussion

The main damage mechanism that leads to the failure of solder interconnect is the initiation and propagation of the fatigue crack. Figure 14 represents the top view of quarter symmetry model for which accumulated plastic work per cycle and characteristic life are calculated. Figures 15 and 16 show maximum accumulated

Table 4 Crack growth constants for 1.0 mil

Constant	Value
K_1	56,300 cycles/psi^{K1}
K_2	−1.62
K_3	3.34×10^{-7} in./cycle/psi^{K4}
K_4	1.04

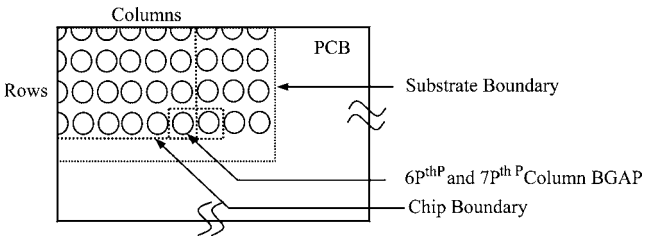

Fig. 14 Top view schematic of the quarter symmetry assembly

plastic work per cycle for each solder interconnect in PC and ATC, respectively. For both cases, solder interconnects near the end of the die accumulate higher plastic work per cycle. It is well known die shadow effect that is the resultant of coefficient of thermal expansion (CTE) mismatch between die/PCB area and bare substrate/PCB area. In a detailed observation, we see that for first, second, and third rows as the distance from neutral point increases $\Delta W_{\max}$ increases until the solder joint at the end of the chip. In the fourth (or the outermost) row, although the inner solder balls show different trend, the sixth and/or seventh solder ball has the largest value in $\Delta W_{\max}$. With an increasing amount of maximum accumulated plastic work per cycle in a solder ball, the possibility of that solder ball failing under fatigue increases. From Eqs. (5) and (6), we see that thermal cycles to crack initiation increases with decrease in $\Delta W_{\max}$ and characteristic solder joint fatigue life is inversely proportional to crack propagation rate per

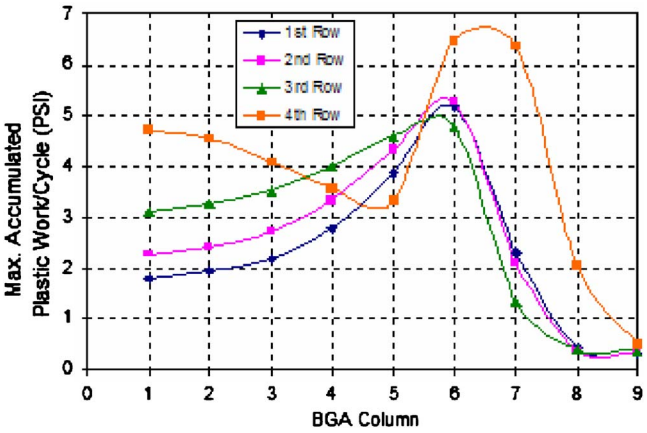

Fig. 15 Power cycling—maximum accumulated plastic work/cycle (PSI) for solder interconnects

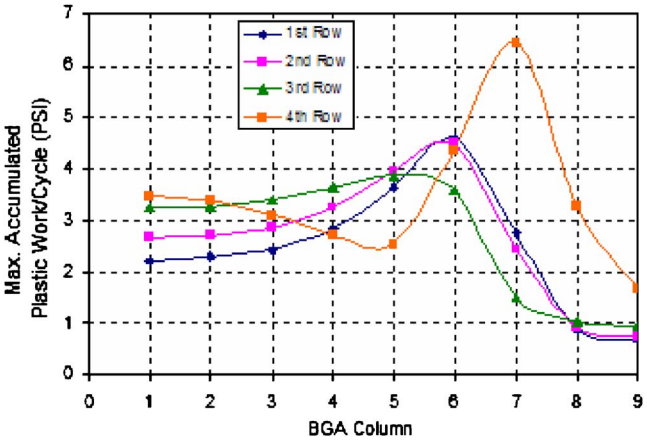

Fig. 16 ATC—maximum accumulated plastic work/cycle (PSI) for solder interconnects

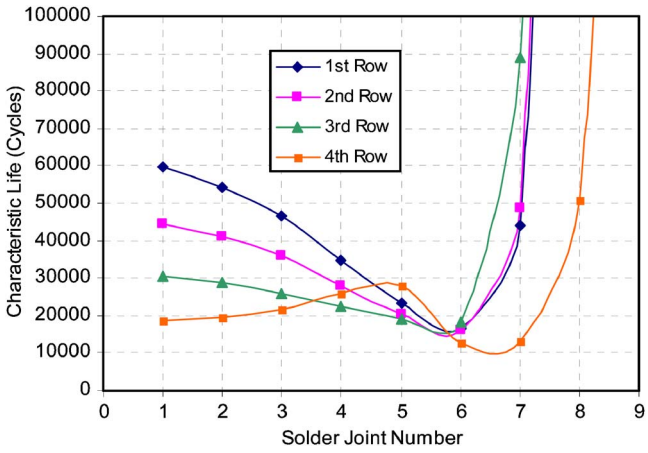

Fig. 17 Power cycling—characteristic life of solder interconnects

thermal cycle. This can be observed in Figs. 17 and 18 where the sixth and/or seventh solder ball in the outermost row has the lowest value in α. The trend matches well with other works, which deal with flip chip PBGA packages. Specifically, Verma et al. [5] predicted the same trend using maximum plastic strain in a solder ball. For a two-parameter Weibull failure distribution for mean cycles to failure ($N_{63.2}$) for a component, the reliability prediction is given by Eq. (8)

$$R = \exp - \left(\frac{N}{N_\alpha} \right)^\beta \tag{8}$$

where β=2.6–4.0; R is the reliability, and N is the number of cycles to achieve that reliability. The two parameters are N_α (the characteristic package life), and β (the shape parameter or Weibull slope). For a series of joints connected electrically, the overall reliability of all the joints is given by the product of the reliability of each joint in the series. As shown in Table 5, power cycling simulation produces a shorter life as compared to accelerated thermal cycling for organic flip chip packages.

With the characteristic life of each joint computed from the finite element calculations, the cycles-to-failure versus reliability relationship can then be generated for any assumed shape parameter. So the shape factor, β, was assumed to be 2.6 and it is noted that failure life increased with the bigger value of β. It is out of the scope of this work to evaluate which β value is appropriate, since we are comparing relative life between PC and ATC. Thus

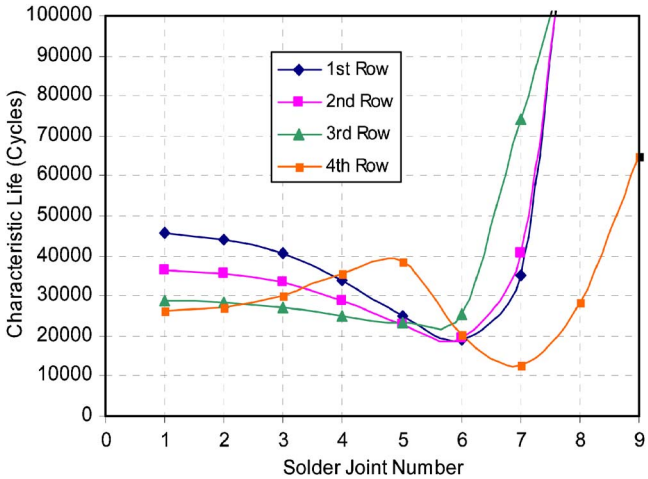

Fig. 18 ATC—characteristic life of solder interconnects

Table 5 Number of cycles to failure for flip chip PBGA package

Package	% Failure	Beta (β)	Power cycling	ATC
Organic	N50	2.6	3207	3720

from the results, we can infer that certain organic flip chip packages are subjected to more severe conditions under power cycling than in the case of accelerated thermal cycling. This is primarily caused by temperature gradient and the thermal expansion mismatches between the package and PCB. The thermal expansion is contributed by the product of the CTE and temperature difference for each component.

Conclusion

The importance of the Power cycling analysis for the qualification of a PBGA package was addressed. A proper and accurate method of simulation was proposed. With careful modeling and correlation, the fatigue life of solder joints of identical geometry can be predicted accurately through empirical relationships under different environmental test or field use conditions. Fatigue Life Prediction proved that Power Cycling could be more severe than ATC for a certain Organic Flip Chip Packages. For the qualification of a PBGA package, it is advised to compare the difference in the acceleration factors between ATC and PC for the proper and safer life projection of the assembly.

Nomenclature

B = transient creep coefficient
G = shear modulus
V = volume of each element
N_o = thermal cycles to crack initiation
a = solder joint diameter
$Cp, mp, K_1, K_2, K_3, K_4$ = constants
da/dN = crack propagation rate per thermal cycle

Greek Symbols

α_{sub} = substrate coefficient of thermal expansion (CTE)
α_{pcb} = printed circuit board CTE
γ = shear strain
ΔT = temperature across package
ΔT_{sub} = temperature variation across substrate
ΔT_{pcb} = temperature variation across printed circuit board
ΔW_{ave} = average viscoplastic strain energy density accumulated per cycle for the interface elements
ΔW = viscoplastic strain energy density accumulated per cycle for each element
α = characteristic solder joint fatigue life

Subscripts

PCB = printed circuit board
SUB = substrate
ATC = accelerated thermal cycling
PC = power cycling

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