Development of Inclined Conductive Bump for Flip-Chip Interconnection

Ah-Young Park, Seungbae Park, and Choong D. Yoo

Abstract—In this paper, inclined conductive bumps (ICBs) are proposed as a substitute for the anisotropic conductive film (ACF). The new interconnection method ICBs can provide controlled bump deformation, uniform electrical conductivity, and fine pitch interconnection without short circuit. The ACF is widely used in the chip-substrate bonding process in today's display and semiconductor industries. This is due to the fact that the ACF has various advantages, such as low bonding temperature, low cost, and small packaging sizes, when compared with those of wire bonding. However, as the bump pitch decreases, the short-circuit problem can occur by lumped conductive particles of the ACF between adjacent bumps. In addition, the electrical conductivity of package varies due to the number of the trapped ACF particles between bonded bumps. Various alternatives, such as coating a thin insulating layer at the outside of the particle and utilizing an array of metal pillars instead of the random distributed particles have been attempted to overcome these shortcomings of the conventional ACF. As another alternative, the ICBs, which are the inclined and hollow copper bumps directly fabricated on electrodes, are suggested. In addition, in this paper is the finite element analysis, which has been conducted to predict the elastic–plastic deformations of the ICBs and their reliability issues. Then, the fabrication processes of the ICB is explained. In such process, the ICBs are fabricated on a test wafer with the inclined angles of 70° and 80°. The ICBs are selectively formed on a target pad at a pitch of 30 μm. A singulated chip with ICBs is assembled on an organic substrate using thermo-compressive bonding. After bonding, the ICBs show reasonable contact resistances of 12–27 mΩ.

Index Terms—Anisotropic conductive film (ACF), Cu conductive bump, electronic packaging, inclined conductive bump (ICB).

I. INTRODUCTION

ANISOTROPIC conductive film (ACF) composed of an adhesive resin and fine conductive fillers, such as metallic particles or metal-coated polymer balls, are key materials for fine pitch chip-on-film and chip-on-glass Liquid-Crystal Display packaging technologies and semiconductor packaging applications [1]. In general, the conductive particle consists of a 3–5-μm diameter polymer core ball coated with nickel
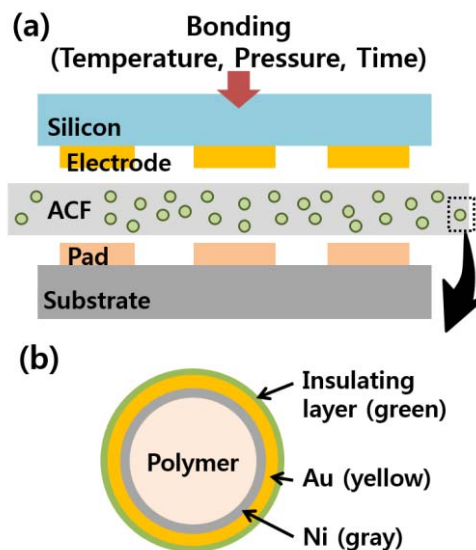
Fig. 1. Schematics of (a) anisotropic conductive film bonding process and (b) ACF conductive particle.

and gold layers. These particles are randomly distributed in an adhesive resin, as shown in Fig. 1(a). The contact between the conductive particles and pad of the substrate is the main electrical conduction mechanism in the ACF interconnection [2]. The ACF has various advantages, such as low-temperature bonding, low cost, and small package size, compared with the wire bonding. In reliability perspective, electronic packages with the ACF have long fatigue life due to its lack of intermetallic compound formation, but comparatively an abundance of the solder based packages. Especially, the ACF shows elastic recovery by inner core polymers of the conductive particle, which are designed to have high elasticity. In addition, as thermo-set adhesives around the particles start to cure, it helps to lock them to maintain the interconnection stability. These can make the package guarantee to have high reliability in the standard 85 °C/85% Relative Humidity test [3], [4]. However, applications of the ACF in the high-density packaging are limited because of the electrical shorts, between adjacent electrodes, formed by random distribution of the conductive particles [5]. To avoid the electrical shorting through the connection with neighboring particles, the conductive particles with nickel-gold plated layers are coated again with a final 10-nm insulating layer, as shown in Fig. 1(b) [6]–[9]. This insulating layer helps to prevent electrical shorts of adjacent particles, and it is designed to become soft when subjected
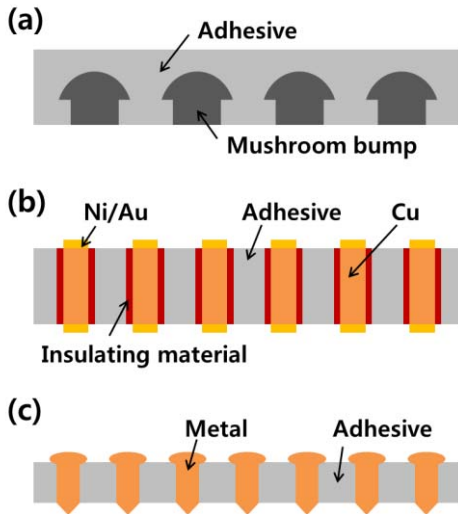
Fig. 2.	Alternatives for ACF. (a) Mushroom-shaped Ni–Au bumps. (b) Cu pillars. (c) Pyramidal Ni over-plating pillars.

to thermal compression during bonding [10]. Furthermore, multilayer ACFs have been proposed to improve the shorting problem. It consists of two layers. The bottom layer contains the conductive particles lying against the substrate, and the upper layer, which is made of a compatible adhesive with the bottom layer, faces the devices. However, the upper layer does not contain conductive particles. Furthermore, the upper layer is designed to have lower viscosity during the bonding process [11], [12].

In addition to the conductive particle, many kinds of vertical interconnection approaches, using structured z-axis conductive bumps, have been developed to improve the problems. These problems include random distribution of the particles, flow of the adhesive during bonding process and electrical short-ing of the conventional ACF. As alternatives, electroplated pillars or nanowires are used for the interconnection. Fig. 2(a) shows mushroom-shaped Ni–Au conductive bumps proposed by the electroplating process on a metal sheet [13]. Another conductive bump has cylindrical shape with a thermoplastic adhesive that is fabricated by nickel over-plating as represented in Fig. 2(b) and (c) [14]–[18]. One advantage of using the conductive bump is that every single dimensional variable, such as bump diameter, height, and pitch, can be controlled during the fabrication process if necessary. Various dimensions of the conductive bumps, which have 10-μm diameter, 6-μm height to 50-μm diameter, 150-μm height, have been studied [13]–[19]. Nanowires within the anodic aluminum oxide template also can be a solution as a substitution for the ACF [20].

In this paper, a new approach to produce the inclined conductive bump (ICB) with inclined and hollow cylindrical shape on a full wafer, is proposed. The ICBs have many advantages that can improve the conventional ACF issues. First of all, contrary to the other fabrication processes of the conductive bumps, the ICB fabrications are very simple. The processes are sequentially composed of an inclined UV lithography, a sidewall seed layer deposition, an electroplating, and a wafer-level chemical–mechanical

polishing (CMP) process. The proposed fabrication processes for the ICB are not required to remove the seed layer using an etching process after the electroplating. Instead of the etching, a CMP process of polishing the seed layer is applied for electrical insulation of each bump. Details of the fabrication process are explained in the next chapter. The fabricated ICBs obtain fine pitch interconnections under relatively low pressure, which can be low as that of the ACF. In addition, there is no electrical short problem due to the predictable deformed direction and amount, since the ICB is inclined toward one direction with a certain angle. Moreover, higher reliability of ICBs is expected compared with that of the conventional vertical solid conductive bumps. That is, because the hollow is filled with adhesive resin, can make elastic recovery similar to that of the ACF. The elastic recovery is simulated using the finite element (FE) analysis. Furthermore, the results of ICBs are compared with those of an inclined solid bump under the appropriate loading conditions to study their differences in the simulation. Finally, a singulated chip with ICBs is assembled on an organic substrate using thermo-compressive bonding, and electrical tests are conducted for measuring total and contact resistances using the Kelvin structure. The ICBs show reasonable contact resistances of 12–27 mΩ.

II. SIMULATION AND EXPERIMENTS

A. Modeling

To numerically investigate the elastic recovery, stress analyses of the ICB are performed using commercially available FE-based program, ANSYS 14.0. The model of a 3-D unit cell of the ICB is a simplification based on the inclined angles. The unit cell contains an organic substrate (1000-μm thickness), an ICB (20-μm height), and a silicon chip (700-μm thickness), as shown in Fig. 3. The detail dimensions are summarized in Table I. The ICB has a hollow cylindrical shape with 20-μm diameter, 20-μm height, and 3-μm thickness. Two types of the ICB are considered depending on its inclined angles of either 80° or 70°, as shown in Fig. 3(a) and (b). In addition, nonconductive film (NCF) placed between the silicon chip and substrate as an adhesive, is considered in FE models, as shown in Fig. 3(c) and (d).

Material properties used in the simulation are listed in Table II. Temperature-independent properties are used for all materials, since only pressure is applied to the model as a loading condition without any change of temperature in this simulation. In the actual bonding process, temperature increases up to 80 °C–100 °C to melt the NCF and assemble the substrate and silicon chip. However, the temperature is relatively low compared with the maximum temperature of operation or reflow process. Therefore, in this simulation, the temperature effect can be ignored. Elastic–plastic properties for copper are used with a bilinear isotropic hardening material model with Young's modulus 128.9 GPa, tangent modulus 650 MPa [21], and yield strength 250 GPa. For the other materials, only elastic properties are implemented. The sym-metry condition is applied at all cross sections, and y-axis

TABLE I
GEOMETRY DETAILS

Item	Dimension (μm)
Substrate	80° - 30(L)×33.5(W)×1000(H) 70° - 30(L)×47.3(W)×1000(H)
Silicon Chip	80° - 30(L)×33.5(W)×700(H) 70° - 30(L)×47.3(W)×700(H)
ICB	20(Dout)/ 14(Din)/ 20(H)/ 50(P)

(L, length; W, width; H, height; P, Pitch; D_{out}, outer diameter; D_{in}, inner diameter)

TABLE II
ELASTIC AND PLASTIC MATERIAL PROPERTIES FOR MODELING

	Substrate	Silicon	NCF	Copper
Young's Modulus (GPa)	22.2	162.7	8.6	128.9
CTE (ppm/°C)	16	3	50	17
Poisson's ratio	0.3	0.278	0.4	0.34
Tangent Modulus (MPa)	-	-	-	650
Yield Strength (GPa)	-	-	-	250

degrees of freedom (UY) of the bottom node of the unit cell are fixed to prevent rigid body motions. With respect to the loading conditions, loading–unloading steps are applied to mimic the bonding process, which is controlled by pressure changes from 1.1 MPa to 0 Pa, respectively. The values come from a calculation of applied maximum force for bonding, 70 N, over a singulated chip area, 8 mm × 8 mm.

The contact boundary condition is assigned at the interface between the top of the ICB and contacted area of the organic substrate. The bottom of the ICB is fixed with the silicon chip, since it is directly fabricated on the silicon wafer. The top surface of the ICB is chosen as a target surface (TARGE169) and corresponding surface of the top substrate is assigned as a contact surface (CONTA172). Augmented Lagrange method with normal penalty stiffness 1.0 and penetration coefficient 0.1 is used for normal contact. Tangential contact is assumed as frictionless. Mesh density, meshing shape, and contact boundary condition are represented in Fig. 4.

To investigate a role of the hollow shape as compared with the filled shape of inclined solid bump, a unit cell of an inclined solid bump is modeled. It has the same dimensions with the ICB, but inside of the inclined solid bump is filled up with copper. According to prior arts, 1.96 to 48 MPa bonding pressure are used for solid bumps [13]–[18], therefore, the minimum value 1.96 MPa is chosen as bonding pressure in this simulation for the inclined solid bump. In this comparison, analysis of only 70° of inclined angle is conducted for its quantitative assessments.

B. ICB Fabrication Process

Recently, the pitch of the bumps or electrodes tends to decrease below 50 μm [5]. Responding to the recent trends, the pitch of the ICB is decided to be 30 μm. The detail manufacturing processes of these ICBs are described below and Fig. 5 shows the fabrication sequence. When compared with the conventional electroplating process of fully filled solid bumps, as listed in Fig. 6, the proposed fabrication process is very simple. This is a wafer-level process. The dimension, 20-μm diameter, 20-μm height, and 3-μm thickness with two inclined angles, 80° and 70°, of the ICB is the same as that of the simulation model.

1) *Electrodes Patterning:* Lift-off process is used for patterning Cr/Au electrodes on a silicon wafer with oxidation. Lift-off process has a representative

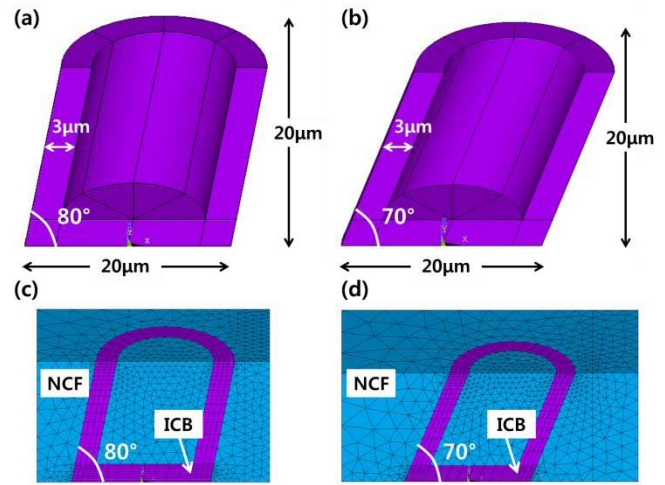

Fig. 3. Schematics of ICB with (a) 80°, (b) 70°, (c) 80° with NCF, and (d) 70° with NCF.

advantage, which is not to conduct complicated etching process. First of all, positive photoresist, AZ9260, is spin-coated on the wafer with 2000 r/min for 50 s, and baked at 110 °C for 2 min 30 s. At this step, thickness of the photoresist is not important for the lift-off process. To make electrode patterns, the conventional UV lithography process is conducted for 30 s under 300 mJ/cm² on the whole wafer. Then, it is developed in the developer solution, AZ400K, for 6 min. Through this step, only the target areas, where electrodes are desired, are eliminated, as shown in Fig. 5(a). After the lithography step, O₂ plasma process is applied for 2 min under 50 W to remove residual photoresists.

2) *Electrodes Deposition:* E-beam evaporator is used to deposit Cr/Au as electrodes on the patterned photoresist wafer with 200 Å/2000 Å thicknesses, respectively. The Cr layer acts as an adhesion layer because of poor adhesion between the Au layer and SiO₂ of the substrate. After the evaporation step, the deposited photoresist is removed by acetone. Finally, only Cr/Au patterns are obtained as electrodes on the target area of the wafer, as shown in Fig. 5(c).

3) *Bump Patterning:* Positive photoresist, AZ9260, is spin coated again on the electrodes with 500 r/min for 50 s.
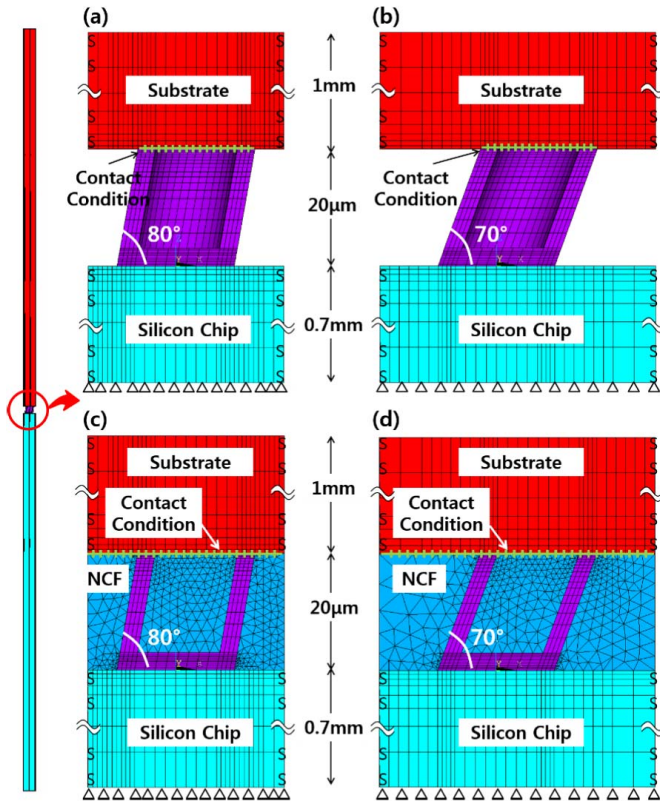
Fig. 4. FE models with meshing and boundary conditions (a) 80° without NCF, (b) 70° without NCF, (c) 80° with NCF, and (d) 70° with NCF.

At this point, an edge bead can be formed around the wafer edge due to the low-spin revolution per minute. When it is formed, it can stick to the mask or cause an unexpected proximity-gap during the second UV lithography process. If the spin revolution per minute is abruptly increased from 500 to 1500 r/min for 0.5 s at the last minute of spin coating, the problematic formation of bead can be resolved. Following the photoresist deposition, the wafer is baked at 90 °C for 3 min. To make inclined hole patterns array, second UV lithography is conducted on the wafer, which is installed on the tilting stage, for 50 s (500 mJ/cm^2), as shown in Fig. 7. Finally, the exposed photoresist is developed in AZ400K for 6 min. O$_2$ plasma process is also applied for 2 min under 50 W to remove residual photoresists. In the inclined lithography step, the relationship among the incident angle (θ_i), reflection angle (θ_r), and refraction angle (θ_t) is determined by the law of reflection and law of refraction, Snell's law, as follows:

$$\text{Law of reflection} : \theta_i = \theta_r \tag{1}$$
$$\text{Law of refraction} : n_i \cdot \sin\theta_i = n_t \cdot \sin\theta_t \tag{2}$$

where n_i and n_t are the refractive indices of the incident and transmitting layer, respectively, and $n_i = 1$ and $n_t = 1.695$ in this paper.

4) *Seed Layer Deposition:* E-beam evaporator is used again to deposit Ti/Cu seed layers with 1000 Å/1500 Å thick-
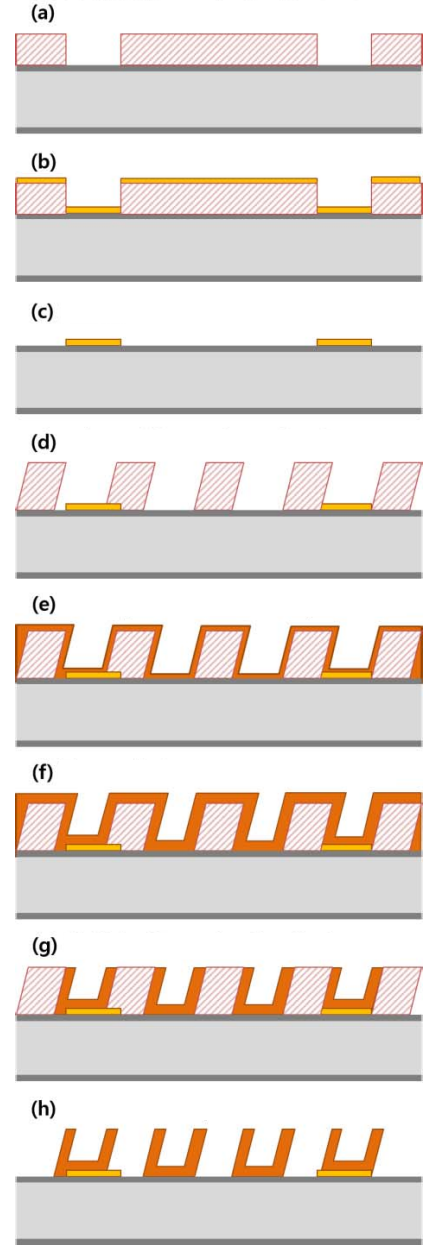

Fig. 5. Proposed ICB fabrication processes. (a) First UV lithography for electrodes. (b) First deposition of Cr/Au electrodes. (c) Lift-off. (d) Second UV lithography inclined. (e) Second deposition of seed layer on PR. (f) Electroplating. (g) CMP for removing top surface. (h) Removal of deposited PR.

ness on the top surface as well as on the inclined sidewall of hole patterned photoresist layer. Ti layer serves as an adhesive between the Au and Cu layers because of poor adhesion between Au and Cu. The seed layers are deposited on the top and sidewall of a whole wafer, and then this Ti/Cu deposition makes electrical connection of the top and sidewall through the whole wafer, as shown in Fig. 5(e). This connected layer acts as a cathode for the next electroplating process.

5) *Electroplating and CMP Process:* The holes do not need to be filled up completely with copper by electroplating. It is only necessary for 3–5-μm thickness of Cu from the seed layer in the electroplating process.

TABLE III
FOUR CASES FOR THE SIMULATION

Case	Inclined Angle	NCF	ICB		Inclined Solid Bump	
			Max. Stress (loading)	Max. Stress (unloading)	Max. Stress (loading)	Max. Stress (unloading)
1	80°	No	62 kPa	0.09e-3 Pa	-	-
2	70°	No	191 kPa	0.20e-3 Pa	284 kPa	233 Pa
3	80°	Yes	16 kPa	516 Pa	-	-
4	70°	Yes	22 kPa	650 Pa	42.8 kPa	230 Pa

The electroplating is conducted for 3-μm thickness under 1000 mA, pulse ON/OFF 40/60 μs, 10 min and 1500 mA, dc 4 min, and electroplating time will increase as thickness of copper layer increases. Finally, CMP process is performed for electrical insulation of connected bumps by polishing the top surface, as shown in Fig. 5(g). The conventional electroplating sequence of the etching and CMP steps are represented in Fig. 6(h) and (i).

6) *Photoresist Removal:* After dipping in acetone, the residual of photoresist is removed. Consequently, only ICBs are obtained as inclined cup-shape on the wafer, as shown in Fig. 5(h).

III. RESULTS AND DISCUSSION

A. Results of Simulation

Four cases are conducted to investigate elastic recovery of the ICB, as listed in Table III. The first two models have a substrate, silicon chip, and the ICB. The others additionally consider effects of the NCF, which is used as an adhesive during bonding. The equivalent stress is measured after loading and unloading, respectively. The first two cases of Table III are simulation results of the ICB without NCF. The maximum stress is observed at right bottom side of inclined ICB under loading, as shown in Fig. 8(a). The maximum value is 191 kPa of the 70° inclined ICB, which is much smaller than the yield strength of copper. Hence, plastic deformation has not occurred. As explained previously, the cases 3 and 4 include NCF as an adhesive between the silicon chip and substrate. The case 3 shows the maximum stress at left-top side as 22 kPa of 70° ICB. As shown in Fig. 9, NCF helps to decrease the maximum stress in loading. According to the simulation results, yielding is not a concern within usual bonding force, 50–70 N. In other words, perfect elastic recovery of the ICBs occurs to improve reliability issues, such as misalignment, warpage, and poor interconnection between an electrode and pad, during their operation.

To investigate a role of the hollow shape as compared with an inclined solid bump, analyzes of only 70° of inclined solid bump with/without NCF are conducted. Since the solid conductive bump has larger contact area than that of the ACF and ICB, larger bonding pressure is required to obtain stable electrical contact of bumps in general. In this step, target pad or substrate can be damaged depending on applied pressure. In this simulation, the minimum 1.98 MPa is chosen as bonding pressure as explained previously. Although simulation results show that equivalent stress of the inclined solid bump under loading is smaller than yield strength of copper, stress values are about 150%–200% higher than the results of ICB with/without NCF cases. In addition to loading results, stress is spread over the contact surface of the inclined solid bump with 230 Pa, as shown in Fig. 10, while stress of under unloading cases is concentrated at a point, inside of the ICB with 650 Pa. This widely distributed stress leads rough surface of the bump during operations, and it can cause point-to-point contact between the bump and substrate, which is a main problem of high-contact resistance.

B. Comparison With the Conventional Fabrication Process

ICBs are fabricated on a bare test wafer, and the inclined angles of the ICB are 80° and 70°, using inclined UV lithography. Inclined angles make certain deformation direction of the ICB, resulting in avoiding electrical shorts. The ICBs are relatively easily deformed by bending moment under bonding pressure, and they obtain vertical and horizontal elastic recovery when they are unloaded. In addition, since the ICB has an inclined hollow shape, NCF goes into the hollow during bonding and it acts like a core ball of the ACF to improve to high reliability. To conduct electroplating process, deposition of seed layers, and then lithography, are common steps for electroplating, as shown in Fig. 6(d)–(f). However, in this paper, lithography is conducted prior to depositing seed layers onto the top and inclined sidewall of holes of the patterned photoresist, as shown in Fig. 5(d) and (e). This step makes the seed layer connected electrically along the photoresist, not along the wafer, as shown in Fig. 5(e). This suggested inverse sequence is a key point when compared with the conventional one. In addition, since the ICB has hollow cylindrical shape, the holes do not need to be filled up completely in the electroplating, as shown in Fig. 5(f). Thus, it takes only 15 min to plate to 3-μm thickness of the ICB. Furthermore, the CMP process not only makes the ICBs flat but also
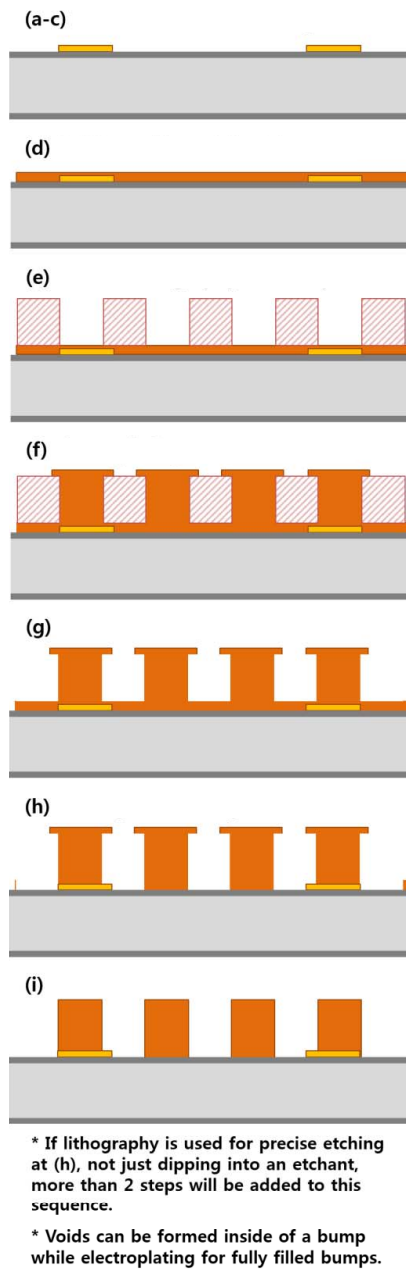
Fig. 6.   Conventional bump fabrication processes. (a)–(c) Processes are the same as in Fig. 5. (d) Second deposition of seed layer. (e) Second UV lithography for bumps. (f) Electroplating. (g) Removal of deposited PR. (h) Etching of seed layer. (i) CMP for flatness.

insulates electrically connected bumps at once, as it removes the top plated layer, as shown in Figs. 5(g) and 11.

On the other hand, vertical conductive bumps are fabricated using the general UV lithography and conventional electroplating. Since the vertical conductive bump stands straightly in z-direction, it obtains only vertical elastic recovery, and the deformation direction cannot be predicted, as shown in Fig. 12. Moreover, it takes more than 2 h to fill up bumps completely, and voids are easily formed inside of the bump due to current density variations during the electroplating. Moreover, bumps are entirely connected to each other along the wafer due to the seed layer, as shown in Fig. 6(f). Therefore, the etching process is essentially required in insulating bumps. For this
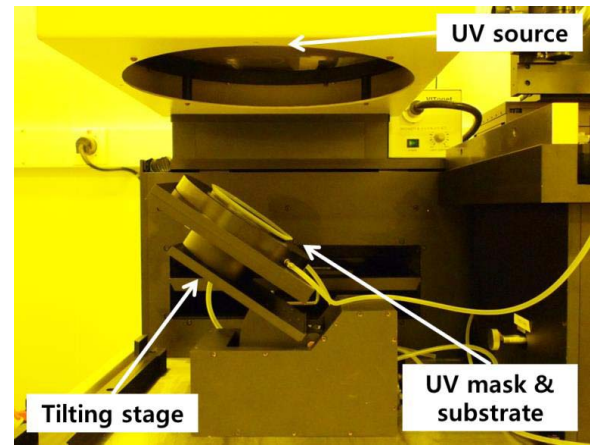

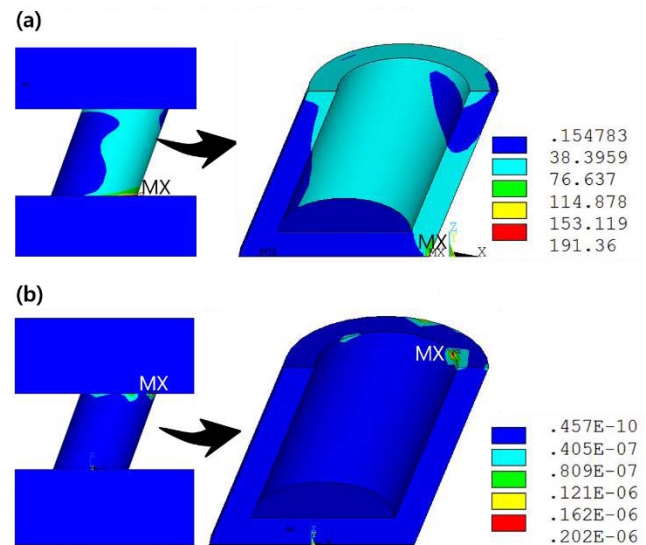Fig. 7.   Inclined UV exposure system.

Fig. 8.   Equivalent stress distribution of 70° ICB without NCF. (a) After loading for 70°, without NCF. (b) After unloading for 70°, without NCF.

step, dipping into an etchant is commonly used, but one or more lithography steps are necessary for obtaining high-precision products and flatness of bumps. This limitations are inevitable and cause high costs and time consumption.

C. Results of ICB Fabrication

Fig. 13 represents a top view of fabricated ICBs with 80° and 70° angle, respectively, having a 20-μm diameter using the proposed fabrication process. It shows the ICBs with 80° have complete hollow shape, but, those with 70° have C-shape. This difference is caused by step coverage during the seed layer evaporation process, as shown in Fig. 14. In case of the 80°, the seed layer is deposited completely up to the inner sidewall. Therefore, perfect inclined cylindrical bumps can be formed by electroplating. On the other hand, the seed layer deposition fails to be covered on the inner sidewall in the case of 70°. Fig. 15 confirms the step coverage problem, as shown in the cross section view of ICBs with each angle. The ICB with 70°, as shown in Fig. 15(b), has inclined L-shape cross section, and it can be clearly compared with inclined cup-shape of 80° ICB, as shown in Fig. 15(a). Consequently, 80° is
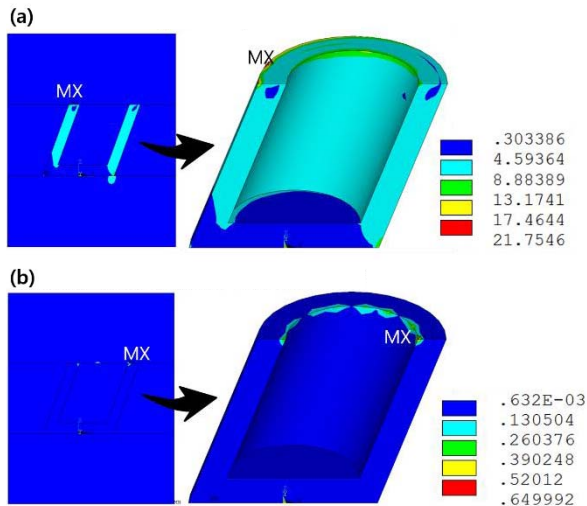
Fig. 9. Equivalent stress distribution of 70° ICB with NCF. (a) After loading for 70°, with NCF. (b) After unloading for 70°, with NCF.
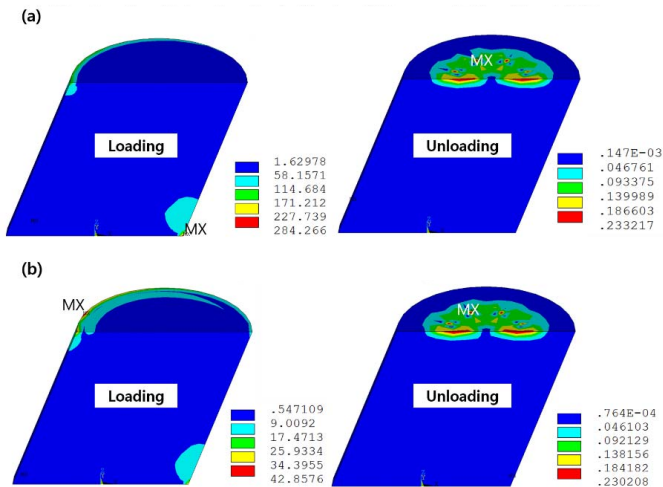

Fig. 10. Equivalent stress distribution of 70° inclined solid bump. (a) Without NCF. (b) With NCF.
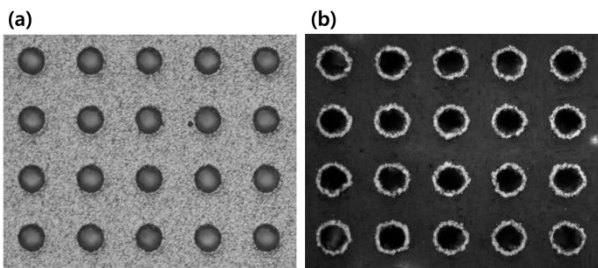

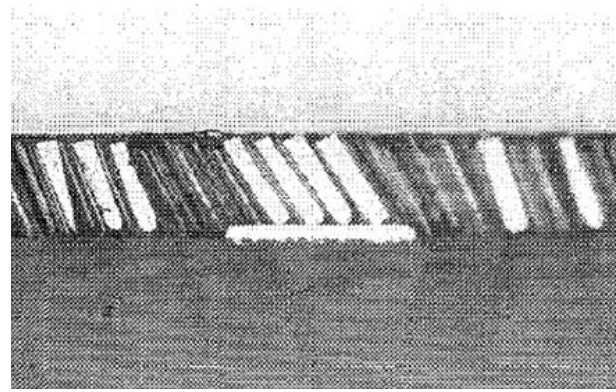Fig. 11. Top view of ICB. (a) Before CMP. (b) After CMP.
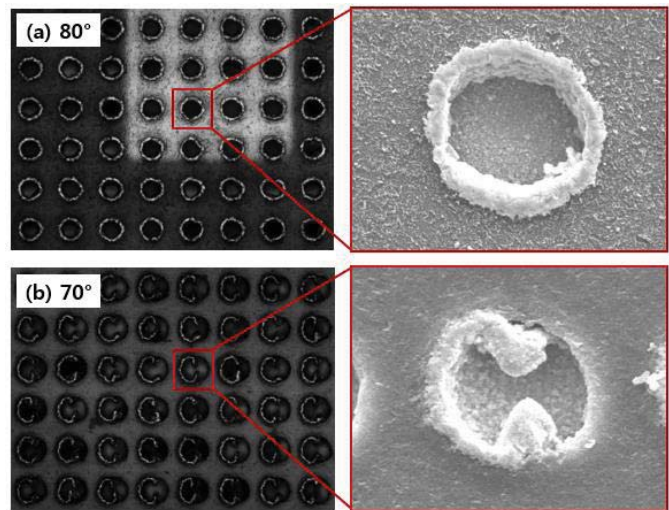

Fig. 12. Collapsed 0.025-mm pitch ACF [14].

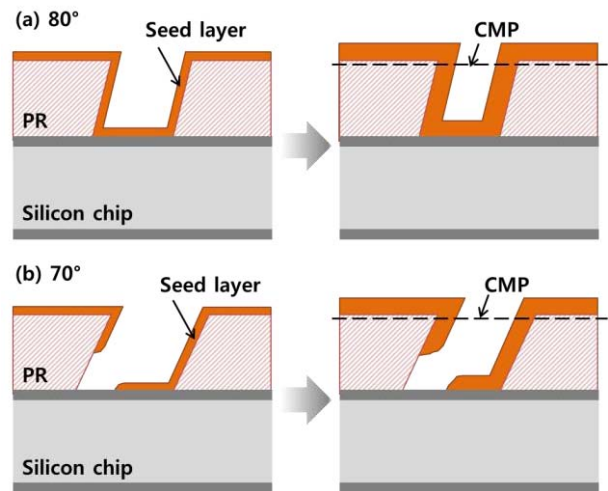Fig. 13. Microscope and SEM images after electroplating of ICB top surface with (a) 80° and (b) 70°.

Fig. 14. Schematics of step coverage during seed layer deposition process. (a) 80°. (b) 70°.

appropriate for the ICBs when a conventional evaporation process is applied in this stage. However, the step coverage problem can be improved if sputtering, physical vapor deposition or inclined evaporation is applied to increase deposition coverage because the only problem is the seed layer deposition at the sidewall. In addition to inclined evaporation, thickness of seed layers can be increased from 1500 to 6000–10 000 Å to maximize coverage possibility as extends the exposure time

of sources. Moreover, electroless plating, which is widely used to plate copper for through silicon vias of high aspect ratio, can be applied to deposit seed layers completely on the ICBs of 70°.
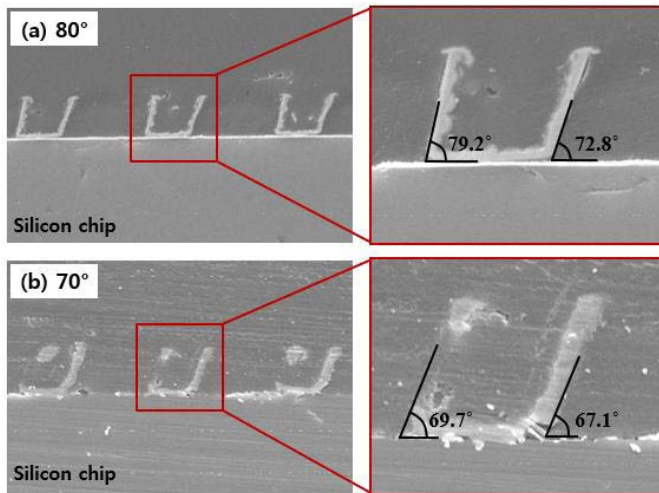
Fig. 15. Obtained inclined angle by inclined UV lithography. (a) 80°. (b) 70°.

Fig. 16. SEM image of ICB.

Fig. 17. (a) Top view and (b) cross section view of fabricated ICB on electrodes.

The inclined angles are observed in Fig. 15, using a scanning electron microscope (SEM). As mentioned in the fabrication process, refractive index of incident medium and transmitting medium, AZ9260, are 1 and 1.695, respectively. Using the Snell law, the incident angles, 17° and 35° are calculated to fabricate the ICBs, to obtain refraction angle 80° and 70°, respectively. As experimental results, 72.8°–79.2° and 69.7°–67.1° are obtained as refraction angles, when incident angles are 17° and 35°, respectively. Excessive thickness and opacity of the photoresist, as well as contaminants on the sample, can result in the errors between the calculations and experimentally obtained angles because they can be an obstacle for UV light to penetrate without scattering.

Fig. 16 shows the final, completed ICBs with 80°, 3-μm uniform thickness, 20-μm height, and 30-μm fine pitch on a wafer. Dimensions, such as diameter and pitch of the ICB, can be adjusted depending on masks used in the lithography process. Although, a film mask, which has minimum pattern size of 15 μm, is used in this paper, a chromium mask can obtain much smaller diameter and pitch. Thickness of the ICBs is also controlled by electroplating time change. Furthermore, photoresist thickness and CMP process decide height of the ICBs, therefore, many types of ICBs can be fabricated to meet various purposes.

D. Assembly and Contact Resistance Measurement of ICB

Total resistances are measured at every 10-N bonding forces from 20 to 70 N to find an optimum bonding force and corresponding resistances. Moreover, contact resistances are measured at 50 and 70-N bonding forces for electrical property of the ICB. Three points, extracted from each of four sides with a total of 12 points, located at the outermost edge of four sides, are measured. Three sets of points extracted from the repeated processes are used to obtain total and contact resistances. 50–70 N is commonly applied for bonding of the ACF. A singulated silicon chip with 80° angle ICBs and organic substrate are assembled with 30-μm-thick NCF using a flip-chip bonder (Finetech). Bonding temperature is 60 °C

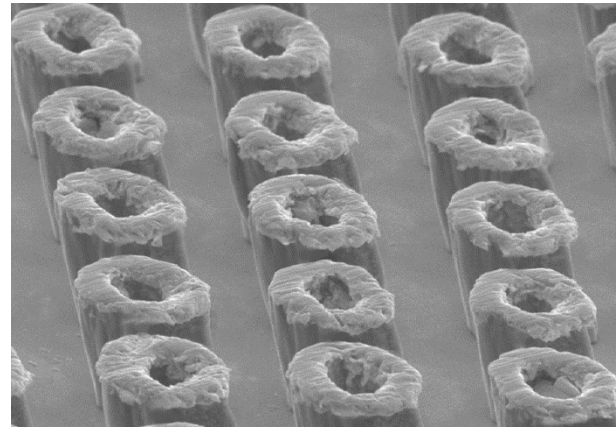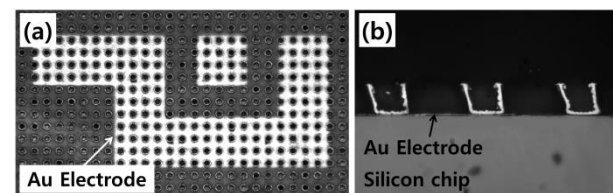for 30 s, and then it increases to 160 °C for 35 s for the chip. However, substrate is maintained at 80 °C continuously. Flowing of the NCF can cause forming voids inside of the cup-shape ICB. In addition, residual NCFs on the top surface of the ICB make its contact resistance high. To avoid these problems, bonding force is constantly applied to the chip until decreasing temperature reaches 100 °C. Fig. 17(a) and (b) shows ICBs fabricated on electrodes and assembled with a substrate for measuring resistances. Especially, top surface of the ICB is observed to be assembled well, without any gap and warpage, with the substrate at 70 N in Fig. 18(b). Total resistances are measured using a digital multimeter, and contact resistances are measured using a four-points probe station (Keithley 236 source measurement unit).

Total resistance results are shown in Fig. 19. Data cannot be obtained at 20 N, since labeling 1, 3, and 4 sides of the assembled chip out of four sides are not connected to the substrate. From 30 N, every side is well connected to the substrate, but it shows high resistance due to insufficient bonding force. As bonding force increases, total resistance tends to decrease. However, there is minimal difference among them beyond 40 N. This result can explain why contact resistances are similar between 50 and 70 N as stated below.

Contact resistances of ICBs vary from 14 to 27 mΩ at 50 N, and their average is 20 mΩ. Similarly, the ICBs have ranges from 12 and 27 mΩ at contact resistances at 70 N whose average is 20.5 mΩ. The minimum contact resistance decreases as bonding force increases, but there is no difference in the average. Contact resistance is easily affected by electrode thickness and calibration of the flip-chip bonder. As thicknesses of ICB plating and electrode, and the number
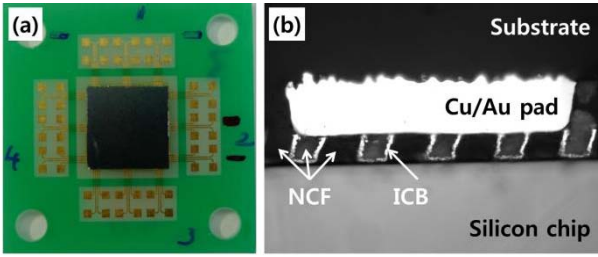
Fig. 18. (a) Top view and (b) cross section view of assembled ICB with substrate.
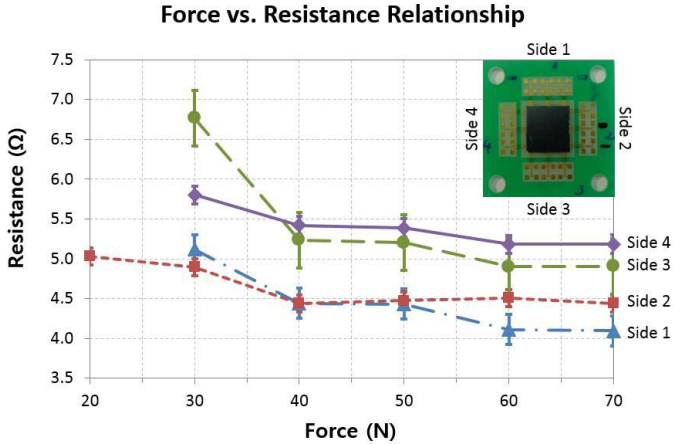

Fig. 19. Measured total resistances with respect to applied forces.

of the ICBs on the electrode increases, contact resistance can be improved. In this paper, 2000-Å thick electrodes are used, which is relatively thin, when compared with that of the conventional electrodes. Thus, when thickness of the Au electrodes increases, electrode resistance will decreases, and it affects the total and contact resistances. In addition to the thick electrodes, ICB thickness can be increased by longer electroplating to reduce the contact resistances of the ICB. About tolerance of the contact resistance, the range of 12–27 mΩ, calibration of the flip-chip bonder is the main reason that makes standard deviation and error of the contact resistance high. As you can observe in Fig. 19, sides 3 and 4 have higher total resistances than the other sides. Especially, side 3 shows wide range of standard error as well. It means that the tip of the flip-chip bonder is not calibrated well enough, which cannot uniformly distribute bonding pressure onto the package. Therefore, when those problems, which are listed in above, are resolved, total and contact resistance of the ICB can drastically decreases with small standard deviation and error.

In prior arts, many different contact resistances of the ACF and conventional/novel conductive bumps in different bonding conditions are reported. The range of the contact resistances of the ACF are distributed from 5–10 mΩ [11] to 2–300 mΩ [22], and their average is about 2–30 mΩ approximately. In addition to contact resistances the ACF, contact resistances of conventional/novel conductive bumps have been published, which have their range from less than 1 mΩ [13] to 15–50 mΩ [18]. The conductive bump shows the relatively low contact

resistances, since it has larger contact surface and cross section area than those of the ACF and ICB. However, the conductive bump is required high-bonding pressure, which can damage other components of package, and it is not suitable for fine pitch packaging because short circuits are easily occurred in case of 50-μm pitch [13]. As a result, when compared with the contact resistance of the ACF and conventional/novel conductive bumps, as well as elastic recovery simulation results and the fabrication process, the ICB still shows competitive contact resistance, and it can be a substitution for the conventional ACF and conductive bumps.

IV. CONCLUSION

In this paper, a new approach about ICBs with novel wafer-lever fabrication is proposed. Experimentally, ICBs are obtained using the proposed processes to improve the problems of conventional ACFs. Furthermore, electrical properties, such as contact resistance and total resistance, are measured using the obtained ICBs. The proposed fabrication processes are low-cost and large-area fabrication. In addition, the obtained ICBs can be applied not only to flip-chip applications but also to 3-D chip stacking.

1) Novel anisotropic copper bumps, ICBs, which are easily dimension-wise controllable, are proposed. In addition, they provide predictable deformation direction, fine pitch, and uniform electronic conductivity. To obtain the ICBs, new fabrication processes are suggested, including inclined UV lithography, electroplating, and CMP process in wafer level. The fabrications have many advantages, such as being more effective, lower cost, and using a simpler process, when compared with the conventional processes.
2) Elastic recovery of the ICB is confirmed using FE analysis. Investigated maximum stress among four cases is much smaller than the yield strength of copper. It means plastic deformation does not occur during loading–unloading, and elastic recovery will perform to improve their reliability.
3) The ICBs are obtained on a test wafer with two inclined angles, 70° and 80°. Their dimensions are 20-um diameter, 20-μm height, 30-μm pitch, and 3-μm thickness. Moreover, it is confirmed that 80° is appropriate for fabrication by cross section views. Plastic deformation does not occur at both 70° and 80°. However, 70° can be used for ICBs when step-coverage problem is solved using sputtering and inclined evaporation, since plastic.
4) Finally, electronic properties, such as contact resistance and total resistance dependent on pressure, are measured for 80° ICBs. They show reasonable values compared with those of conventional ACFs.

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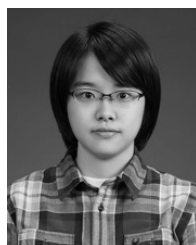
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