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Prediction of deformation during manufacturing processes of silicon interposer package with TSVs

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ABSTRACT

The purpose of this paper is to analyze and predict the thermal deformation of the through silicon via (TSV) interposer package during the manufacturing process and to perform a parametric study to minimize the warpage and thermal stress. Samples were selected during different stages of the assembly to observe the thermal behavior change. The Digital Image Correlation (DIC) technique was employed to measure the real-time deformation of the samples under thermal loading. To make a finite element analysis (FEA) model, material properties were characterized by DIC and Dynamic Mechanical Analysis (DMA). Based on the material properties and deformation data determined by experiments, a validated FEA model was established. To reduce the modeling complexity and the computing time in the simulation, the C4/underfill layer, micro bump/underfill layer, and TSV interposer were assumed to be isotropic. The most effective material properties for the isotropic layers were calculated by the composite theory. Also, the simulation followed the sequential manufacturing processes to investigate the thermal deformation change of each step and to obtain a more accurate prediction result. The thermal behavior from simulation showed a good agreement with the experimental result and this verified simulation model was implemented for the parametric study. A series of simulations were carried out to minimize the package warpage. To avoid any delamination failures, the stresses at the interface between the interposer and underfill were also evaluated. The effect of the interposer underfill material property, substrate material property, substrate thickness, and TSV density (Cu volume fraction) in the interposer were studied. It has been shown that low modulus, low coefficient of thermal expansion (CTE), and high glass transition temperature (T_g) underfill, as well as a low modulus and low CTE substrate can mitigate the package warpage and stress development at the interface between interposer and underfill. Also, a larger Cu volume TSV interposer and thick substrate can lessen the warpage of the package and stress at the interface.

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1. Introduction

The miniaturization and the increasing performance of electronic devices require high I/O, low power consumption, and smaller package dimensions. As a result, three-dimensional (3D) die stacking technology is gaining popularity in the microelectronics industry. The silicon chip has become thinner for the stacking and the number of interconnection pads on the chip has increased. However, the conventional wire bonded substrate cannot accommodate this fine-pitched, high I/O chip. To meet this challenge, the TSV interposer has emerged as one of the most promising technologies [1]. The TSV interposer serves as an intermediate layer redistributing the large array of fine-pitched pads on the chip to the fewer, relatively large-pitched pads on the conventional substrate [2]. Therefore, one or more die stacking is possible by the TSV interposer [3,4]. Moreover, the short electrical interconnect length of TSV is a great advantage because the resistance is decreased, resulting in high signal speed and reduced power consumption. On the other hand, the thin die and interposer are exposed to more warpage during the assembly process due to their low stiffness. The excessive warpage is a critical issue since it not only causes the manufacturing failure such as an open solder joint, but also leads to long term reliability problems like delamination and die-cracking. In addition, the low/k interlayer dielectric (ILD) of interposer is more prone to the delamination failure due to its weak mechanical properties [5,6]. Hence, the thermal deformation of TSV interposer packages has to be taken into account in designing the TSV interposer package.

Thermal deformation has been one of the critical issues in microelectronics packaging for a long time. Verma et al. [7] developed far infrared Fizeau interferometry (FIFI) and shadow moiré with enhanced sensitivity (SMES) for real time measurement of ball grid array (BGA) package.

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Tsai et al. [8,9] also used the Twyman Green interferometer and shadow moiré method to investigate thermo-mechanical behavior of a flip chip BGA during manufacturing process and thermal cycling. They validated the experimental result with FEA and a theoretical solution. Recently, many efforts have been devoted to the reliability study of TSV technology. Some publications are available about the thermal deformation of TSV interposer package [10–12]. However, most of work is concentrating on the numerical study. Experimental verification has to be addressed using a real product. The warpage prediction of multi-stacked package is much more complex than the simulation for the existing package types due to its sophisticated structure. Moreover, it passes through more reflow processes in the course of production, which makes the simulation increasingly difficult to imitate. The purpose of this study is to make a simplified but accurate simulation model, which can estimate the deformation of the TSV interposer package at each stacking process. Also, the material properties are optimized to minimize the warpage and delamination.

In this paper, the authors employed 3D DIC technique to measure the real time deformation of TSV interposer package under thermal loading. Also, the in-plane displacement of a bare substrate, interposer, and Application Specific Integrated Circuit (ASIC) was measured by DIC and used to characterize the CTE. DMA was executed to characterize the modulus of substrate. The 3D FEA was performed to predict the out-of-plane displacement of the package. The effective moduli and CTE were applied to the numerical model for modeling efficiency. The validated simulation model was obtained by comparing simulation and experimental results. Then, this simulation model was utilized for a parametric study. An optimization study was performed to determine the optimum material properties to reduce package warpage and interface stress at the corner of interposer and underfill. The accuracy of the warpage prediction is available by adapting a procedure presented in this study.

2. Experiment

2.1. Sample

The test specimen used for this study is shown in Fig. 1. The package consists of the organic substrate, interposer, ASIC, memories, and stiffener. The interposer is mounted on the substrate with *C*4 bumps and an ASIC and memory chips are connected to the top surface of interposer through micro bumps. The underfill is dispensed to decrease the thermally induced stresses and strains at the joints. The stiffener is attached on the substrate by an adhesive to alleviate the warpage. The interposer has TSVs filled with Cu. The sample dimensions are summarized in Table 1. To measure the warpage during the manufacturing process, four kinds of samples were chosen. The samples used in this study are listed in Table 2, and their manufacturing process is described in Fig. 2. The ASIC is assembled on the interposer first, and then mounted on the substrate together. The interposer and chip stacking temperature during assembly is 245 °C and the stiffener attach temperature is 175 °C.

Table 1
Parts dimensions.

	Dimension (W × L × T)
Substrate	40 × 40 × 1.15 mm^3
ASIC	18.5 × 18.6 × 0.4 mm^3
Memory	8 × 4 × 0.5 mm^3
Interposer	26.4 × 19.5 × 0.1 mm^3

2.2. Material property and warpage measurement

DIC, which is a form of photogrammetry, is a non-contact, full-field optical measurement technique in which both the in-plane and out-of-plane displacement can be computed by the pictures of the target object at initial and deformed stage [13]. This is accomplished by correlating thousands of facets on the sample surface which is considered as a strain gauge. The measurement sensitivity of DIC is dependent on the calibration determined by sample size. In this study, the sensitivity was about 2 μm for the ASIC and 3 μm for the package measurement. The experimental setup was composed of a 3D DIC system, a convection thermal chamber, and a light source. A picture of the setup is shown in Fig. 3. To generate the facet, white paint was sprayed on the sample surface. The images of the sample were taken at every 20 °C in the temperature range from 25 °C to 245 °C and then processed by a DIC program to calculate the displacement. The ramp up speed was 10 °C/min. In case of the package sample, bottom (substrate side) and top surface (die side) were measured respectively to evaluate the overall and die area deformation of the packages. In the top surface measurement, the ASIC warpage was observed. Except for the package sample, the deformation of bottom surface (bump side) was assessed. The warpage is defined by the out-of-plane displacement of two diagonals with respect to various temperatures. As already mentioned, full-field displacement of the target surface was calculated by DIC. Then the out-of-plane deformation along both diagonals was extracted to get the warpage result. The direction of the substrate diagonals is defined in Fig. 1. The substrate diagonal 1 and 2 are not identical due to the interposer, whereas the diagonals of the ASIC, interposer, and combo die are symmetrical. The temperature was recorded from the dummy sample placed near the test sample during the test. The result was used for the validation of the simulation. At the same time, the in-plane displacement of the ASIC, interposer, and bare substrate was measured by DIC for characterizing CTE. The CTE is

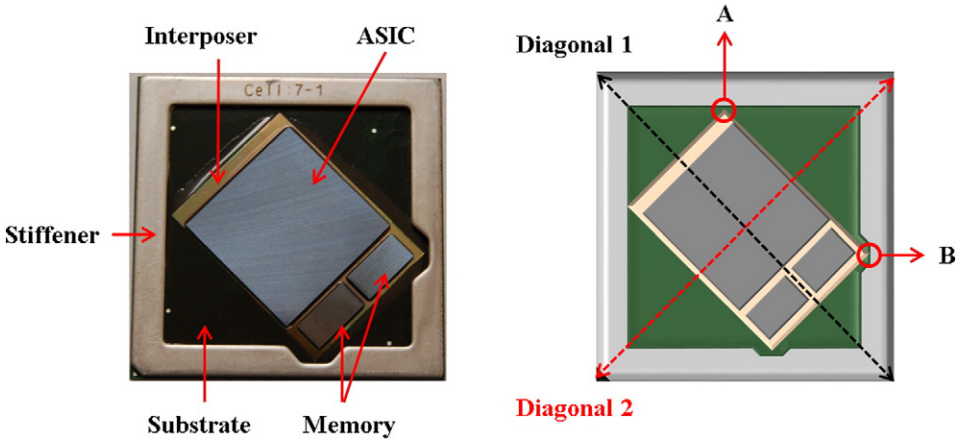


Fig. 1. Test vehicle (TSV interposer package).

Table 2
Test vehicles for warpage measurement.

Sample	Description
ASIC	–
Interposer	–
Combo die	ASIC + micro bump/UF + interposer
Package	Combo die + memory + C4/UF + substrate + stiffener + stiffener adhesive

determined by taking the slope of the strain versus temperature. Fig. 4 presents the CTE measurement result. Also, the modulus of substrate was measured by DMA and the result is plotted in Fig. 5. The substrate was cut in a size of $20 \times 3.8 \times 1.2$ mm^3 (L × W × T) and 0.1% strain was induced by 1 Hz in a three point bending test. For convenience, the storage modulus from DMA was intended to be a temperature dependent elastic modulus. The material properties used for this study are listed in Table 3. Except for the substrate and interposer, other material properties were obtained from company data sheets and literatures.

3. Simulation

The most demanding task in the modeling for TSV interposer packages is dealing with various scales of the detail features in a model. It is impossible to create all TSVs and bumps in 3D model due to several orders of difference in length scales. In the current study, based on the composite theory, the package was considered as a laminated composite, and the C4/underfill layer, micro bump/underfill layer, and TSV interposer are assumed to be a fiber reinforced matrix. By calculating the effective material property for those layers, they were treated as an isotropic material as shown in Fig. 6. This approach can be employed when the purpose of study is to evaluate the overall thermal deformation of the package. Determining thermal fatigue life of solder joints or vias are not in the scope of this study.

To predict the out-of-plane displacement of the flip chip package, Park et al. [15] presented a proper formula for the effective moduli of the solder/underfill layer. They developed the explicit expression for the in-plane and out-of-plane effective properties. An analytical solution was also presented using the classical lamination theory. It was demonstrated that the in-plane effective property ($E^{eff}_{x,y}$ and $\alpha^{eff}_{x,y}$) is the most appropriate for the isotropic material property of the C4/underfill layer. In this paper, in-plane and out-of-plane effective material properties in Ref. [15] were calculated for the C4/underfill layer, micro bump/underfill layer, and TSV interposer. Then those composite layers were assumed that 1) isotropic materials have in-plane effective material property and 2) orthotropic materials have in-plane and out-of-plane effective material properties. The warpage simulation result showed that the error between cases 1 and 2 was less than 1%, which matched the result of Ref. [15]. Therefore, the in-plane effective material property as the isotropic materials was used for the C4/underfill layer, micro bump/underfill layer, and TSV interposer. In Ref. [15], the in-plane Young's modulus is given by

$$E^{eff}_{x,y} = \frac{1}{\left[\frac{c_s}{E_s} + \frac{c_u}{E_u}\right] - \frac{c_s c_u (\nu_s E_u - \nu_u E_s)^2}{E_s E_u (c_s E_s + c_u E_u)}} \tag{1}$$

here, E is Young's modulus, ν is Poisson's ratio, and c is the volume fraction. The subscript s means fiber (C4 bump, micro bump, and via) and the u means the matrix (underfill and interposer). The effective CTE can be expressed as

$$\alpha^{eff}_{x,y} = (1+\nu_u)\alpha_u c_u + (1+\nu_s)\alpha_s c_s - \alpha^{eff}_z \nu^{eff}_{xz} \tag{2}$$

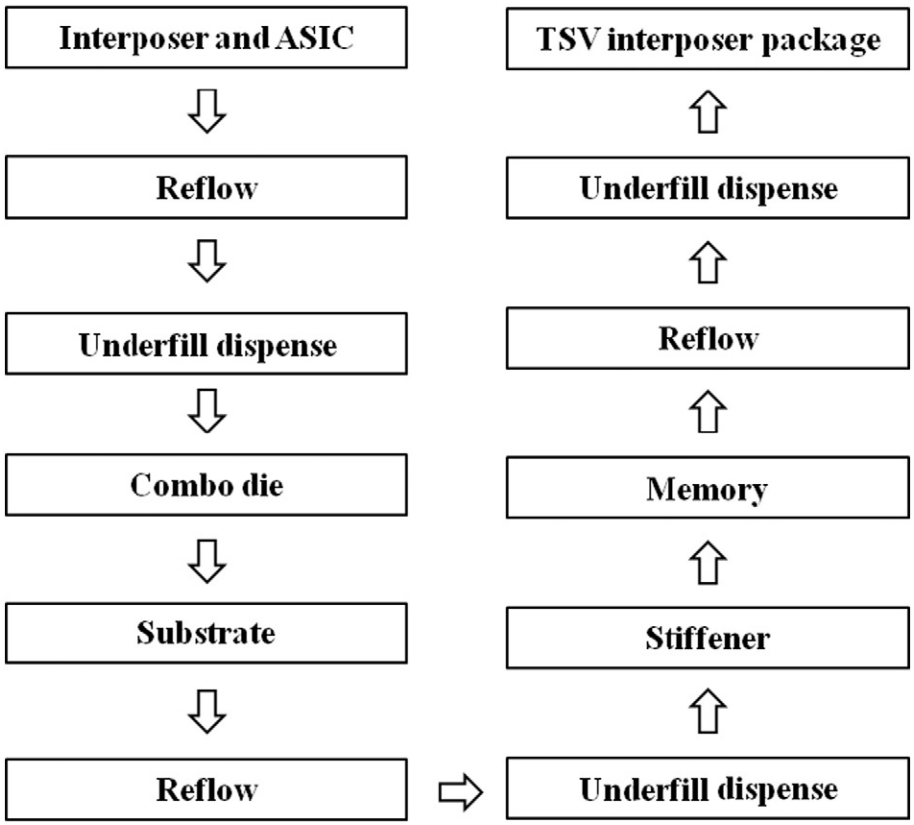


Fig. 2. Manufacturing process.

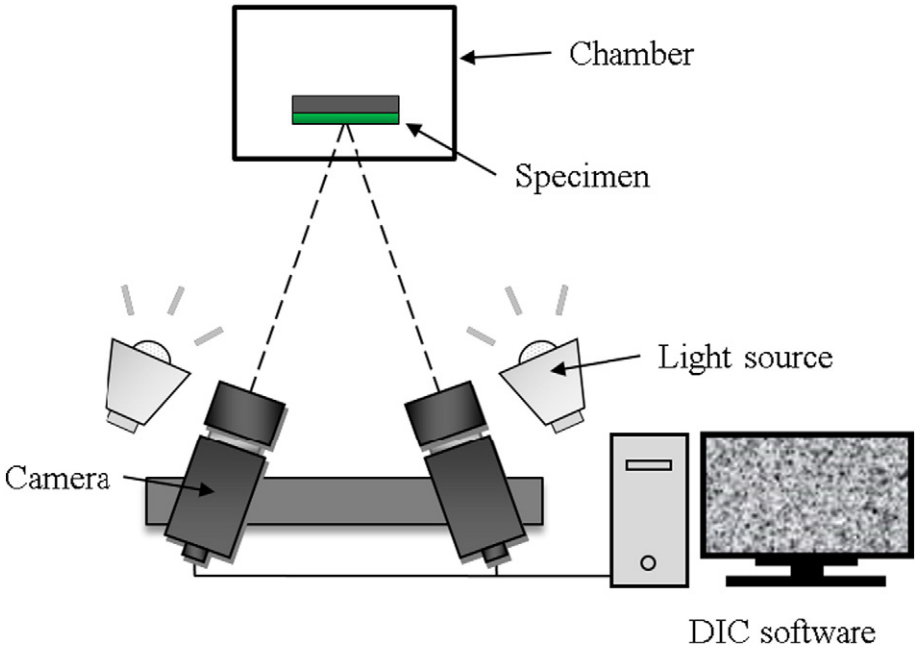


Fig. 3. Schematic of 3D DIC system setup.

where

$$\alpha_z^{eff} = \frac{E_s\alpha_s c_s + E_u\alpha_u c_u}{c_s E_s + c_u E_u} \tag{3}$$

$$\nu_{xz}^{eff} = c_s\nu_s + c_u\nu_u \tag{4}$$

In the case of the interposer CTE, the experimental data was utilized instead of the effective material property. Commercial FEA software, ANSYS (V. 14.5) was used in this study. To take an advantage of the symmetric structure of the sample, a 3D half model was constructed in the simulation as shown in Fig. 7. The 8 nodes brick SOILD185 element was used. To avoid the locking behavior and for an accurate result, at least three layers of elements through the thickness of each material were modeled [16,17]. The center node on diagonal of bottom surface of the substrate was fully fixed to remove the rigid body motion. The symmetry boundary condition was applied at the cross-sectional area. The model is composed of the substrate, *C*4/underfill layer, TSV interposer, micro bump/underfill layer, chips, stiffener, and stiffener adhesive. The whole package was modeled first and components of interest were activated by the element birth and death option [18]. For instance, all components were deactivated except for the interposer, ASIC, and micro bump/underfill, when the combo die was simulated.

4. Result and discussion

4.1. Warpage measurement

Experimental result by DIC with respect to temperature is presented in Fig. 8. In Fig. 8 (a), the warpage of interposer, ASIC, and combo die is described. In this paper, a positive sign of warpage means a convex (smiley) shape of test vehicle, when the bottom surface (bump or solder ball side) of the sample is facing down. The ASIC shows a constant warpage of 10 μm through the temperature range, which means that the chip has a residual deformation. This may be developed during fabrication processes such as a wafer thinning and layer deposition. The interposer exhibits a significant residual warpage more than 100 μm at 25 °C, and the out-of-plane deformation keeps increasing as temperature increases. The severe residual warpage can be explained by its thickness. Since the interposer is much thinner than ASIC, it is more sensitive to the mechanical stresses during fabrication steps. Also, the warpage change by temperature fluctuation represents that the structure of interposer in *Z*-axis is not symmetrical. It has many thin layers on top and bottom surfaces, such as passivation layer and inter-metal dielectric (IMD) layer which have different material characteristics. A thermal deformation of those layers will affect the interposer deformation since the thin interposer has a lower stiffness. After the ASIC and interposer were stacked, the residual warpage reduced. The combo die, which is a combination of ASIC, interposer, and micro bump/underfill layer, shows a constant warpage of 60-70 μm in the specified temperature range. The out-of-plane displacement of TSV interposer package is plotted in Fig. 8 (b). The warpage from the substrate diagonal 1 (long side of the interposer) is bigger in comparison to the substrate diagonal 2 (short side of the interposer). The package warpage decreases linearly as the temperature increases until 180 °C. Above this temperature range, the slope changes since the deformation exhibits a gull-wing shape by the effect of the stiffener. The ASIC warpage on the top side decreases linearly in this heating condition. It should be noted that bare substrate warpage was not observed. Since its structure is symmetric in *Z*-direction, the out-of-plane displacement from previous studies with similar samples was consistent in temperature change and close to zero.

4.2. Simulation result

In order to predict the out-of-plane deformation, the simulation followed the actual assembly process. As analysis is conducted through the manufacturing steps, key findings help to modify the model and increase the accuracy as the previous condition is implemented as the next boundary condition. First, the deformation of the individual samples was identified. Then, simulations for the assembled parts (whole packages) were conducted.

It should be noted that the determination of the stress free temperature (reference temperature or zero-warpage temperature) plays a significant role in the warpage prediction during the assembly process since it affects a value of the maximum warpage at room temperature. In many cases, a single underfill curing temperature is commonly used as the stress free temperature for the whole package model. However, each component of the package can have different stress free temperatures from its own manufacturing condition and the residual strain can

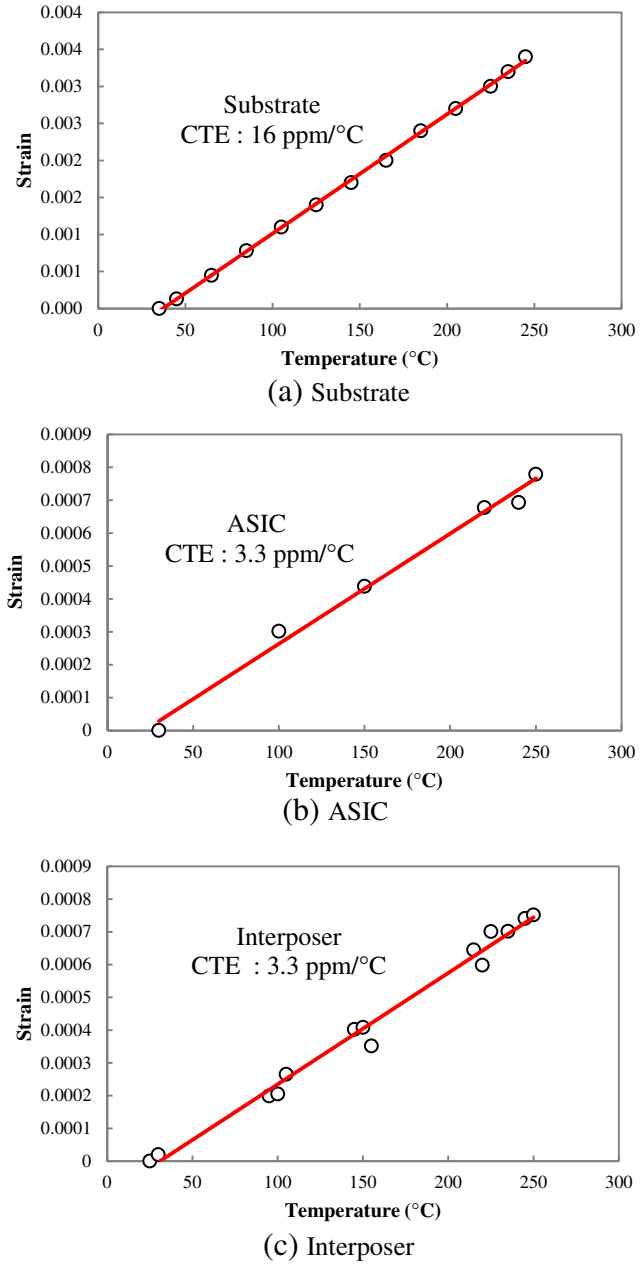


Fig. 4. CTE measurement result.

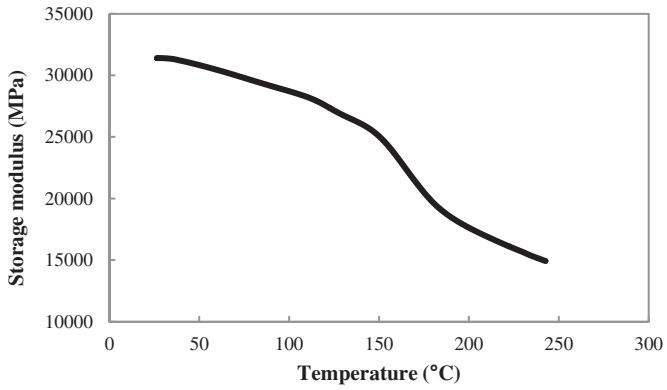


Fig. 5. Substrate modulus measurement result.

Table 3
Material properties.

	Temp. (°C)	E (GPa)	CTE (ppm/°C)	T_g (°C)	ν
Underfill (for interposer)	25	7.9	26	122	0.3
	260	0.2	107		
Substrate	25	31.0	16	–	0.3
	150	25.0			
	180	19.5			
	245	14.5			
Interposer	–	168	3.3	–	0.28
ASIC	–	169	3.3	–	0.28
Memory	–	169	2.6	–	0.28
Cu	–	125	16.5	–	0.3
Underfill (for ASIC and memory)	25	7.5	30	135	0.3
	260	0.1	105		
Stiffener	–	118	17.7		0.3
SnAg	–	−74.995 T + 52,582 [14]	21.5	–	0.4
Stiffener adhesive	0	3.3	20	165	0.3
	245	0.1	55		
Passivation	–	70.1	0.5	–	0.2
IMD	–	270	5	–	0.28

change the warpage free temperature. In the current study, the stress free temperature was determined by observing the slope change of warpage in terms of temperature and the actual process condition.

As seen in Fig. 8 (a), the ASIC shows a small residual strain and does not deform by temperature increase. Therefore, the residual strain was not considered for the ASIC and the bare silicon was used for the ASIC material. On the other hand, the interposer has a significant residual warpage and deforms during temperature change. To generate this residual deformation, 8 μm thick passivation layer was modeled on the bottom side (substrate side) of interposer and 6 μm thick IMD layer and 2 μm thick passivation layer were created respectively on the other side. Then 0.4% in-plane compression strain was applied to the

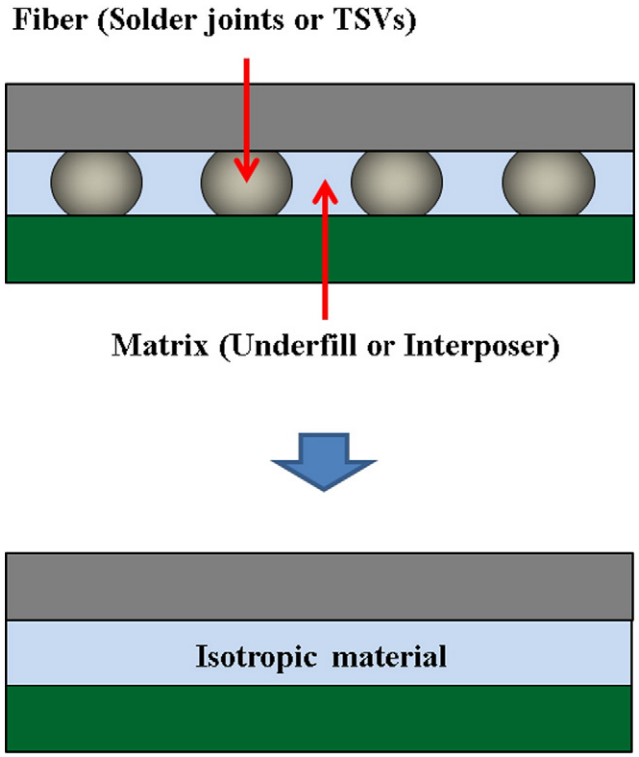


Fig. 6. Simplification of the composite layer by the effective material property.

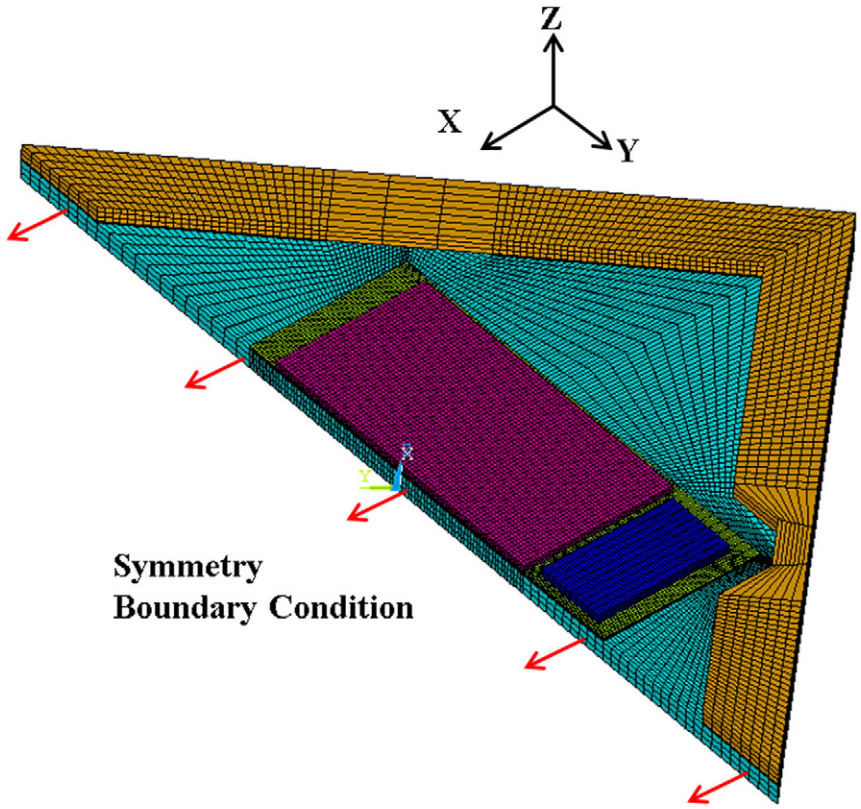
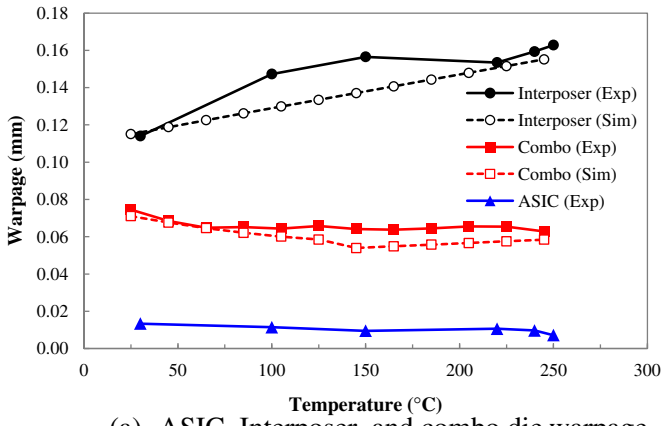
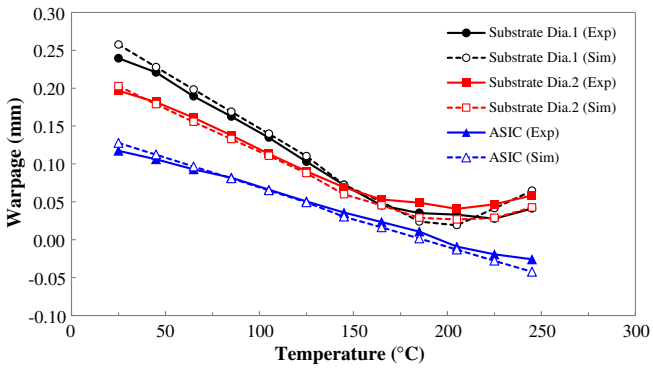


Fig. 7. FEA model.



(a) ASIC, Interposer, and combo die warpage



(b) TSV interposer package warpage

Fig. 8. Warpage comparison between the experimental data and FEA results.

substrate side passivation layer. This initial strain was deduced from a series of simulations using arbitrary strain numbers. The same amount of initial deformation between experiment and simulation was achieved with 0.4% initial strain. The stress free temperature of the interposer including the passivation and IMD layers was to be 180 °C. This was defined based on the process temperature in the previous fabrication stage. The interposer's simulation result is demonstrated in Fig. 8 (a). Then, the combo die having an ASIC, interposer, and micro bump/underfill was analyzed. The conditions from interposer simulation such as stress free temperature and residual strain were used for combo die analysis. The stress free temperature of micro bump/underfill layer was to be 165 °C, which was the underfill dispense and curing temperature. The underfill curing condition was 1 h at 165 °C. In the underfill curing temperature, both solder and underfill exhibit highly viscous characteristics. However, solder creep is constrained by underfill since the volume fraction of solder is about 10% in C4/underfill layer and less than 3% in micro bump/underfill layer. Therefore, overall viscous behavior of effective material is close to viscoelastic characteristics of underfill. The viscoelasticity was not considered in the simulation but the stress of the underfill layer was assumed to be relaxed during the curing process. Thus, the underfill curing temperature was determined as the stress free temperature. Lastly, the ASIC stress free temperature was 180 °C. This result is also plotted in Fig. 8 (a).

After the component level simulation, the analysis for the whole package was carried out. The residual strain and stress free temperature determined in previous simulation were also employed in this analysis. As mentioned earlier, the substrate was assumed to be an isotropic material, consisting of no residual strain. Based on the warpage plot in Fig. 8 (b) and output from simulation, the stress free temperature of the substrate was decided to be 185 °C. Like the micro bump/underfill layer under ASIC, the stress free temperature of C4/underfill layer and micro bump/underfill layer for memory was 165 °C which is the underfill dispensing and curing temperature. The memory stress free temperature was targeted to be 180 °C. The attachment temperature (175 °C) in

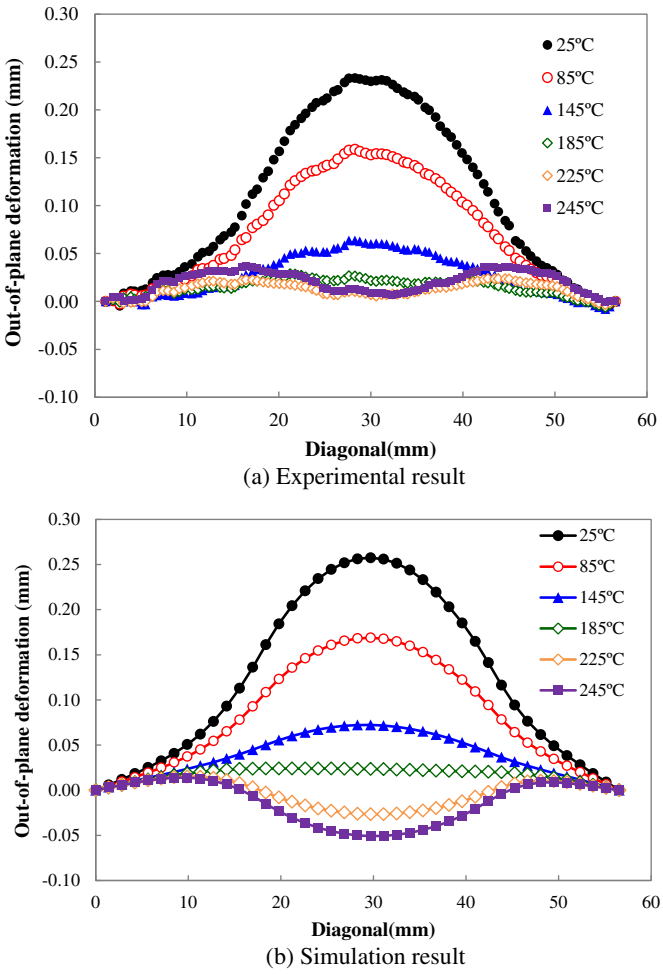


Fig. 9. Out-of-plane deformation of diagonal 1.

the assembly process for the stiffener and the stiffener adhesive was set to their stress free temperature. The result is shown in Fig. 8 (b) and a good agreement has been achieved between the FEA and experimental result. In Fig. 9, experimental and simulation results of diagonal 1 are presented. The results show that the experimental and simulation deformation agree well below 185 °C. However, a discrepancy appears above 185 °C. Above that temperature, both experimental and simulation results exhibit a gull-wing shape deformation due to stiffener. In the simulation, the die area of package sags more at higher temperature.

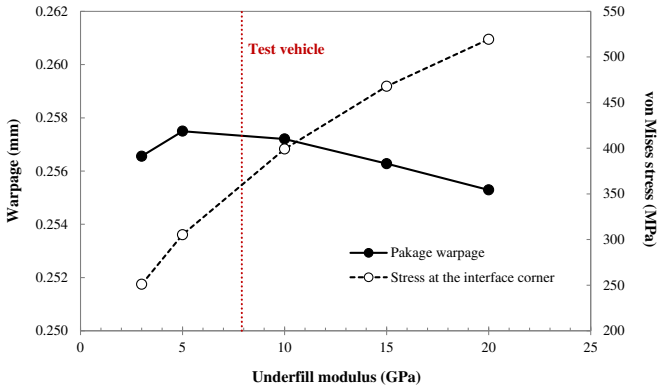


Fig. 10. Underfill modulus impact on package warpage and interface corner stress.

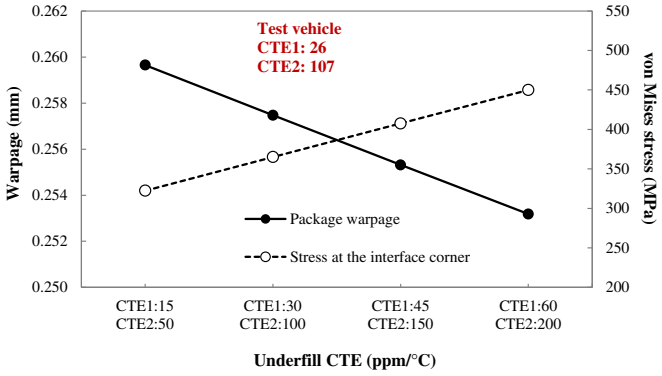


Fig. 11. Underfill CTE impact on package warpage and interface corner stress.

On the other hand, the actual deformation of die area does not shift much above 185 °C and both side areas bulge more as temperature increases. It might be attributed to a buckling of the package because of stiffener. The effect of stiffener needs to be investigated. Another possible reason is a non-linear behavior of package materials with respect to temperature especially substrate. Viscous behavior was not considered in this study. Although some error exists at high temperature range, the simulation model was used for optimization study since the warpage and thermal stress generation was not significant in that temperature range.

4.3. Optimization study

After the verification study of predicting the out-of-plane deformation, the FEA model was employed in a parametric analysis. The primary focus of the optimization was to alleviate the package warpage and the stress at the interface corner. In Fig. 1, two corners of interposer are described. Equivalent stresses at the outermost nodes on interposer-underfill interface and substrate-underfill interface at Point A and B were compared. Since the stress of the node on the interface between the interposer and C4/underfill at Point A was the highest at 25 °C, it was chosen as a parameter to be evaluated. For the warpage evaluation, warpage from diagonal 1 was compared. Material parameters including the elastic modulus, CTE, and T_g of the interposer underfill and substrate were studied. Also the geometric parameters such as substrate thickness and TSV density of interposer were analyzed. For comparison, the warpage and stress level of the test vehicle in the previous section are plotted in Fig. 10 and Figs. 12–16.

Figs. 10–12 show the impact of the underfill material property. In case of the underfill modulus as shown in Fig. 10, a modulus change below T_g was observed. The modulus above T_g was assumed to be 0.1 GPa. The results indicate that the package warpage is not sensitive to underfill material property. The underfill is a compliant layer com-

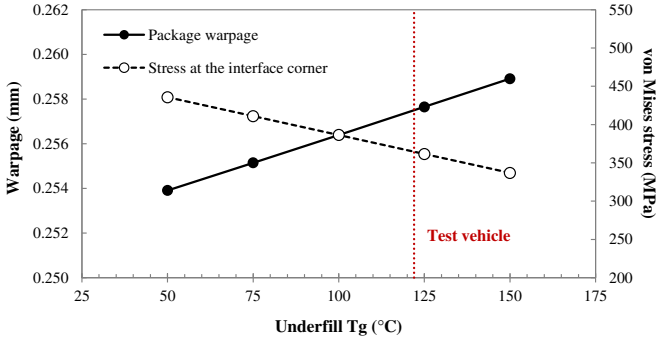


Fig. 12. Underfill T_g impact on package warpage and interface corner stress.

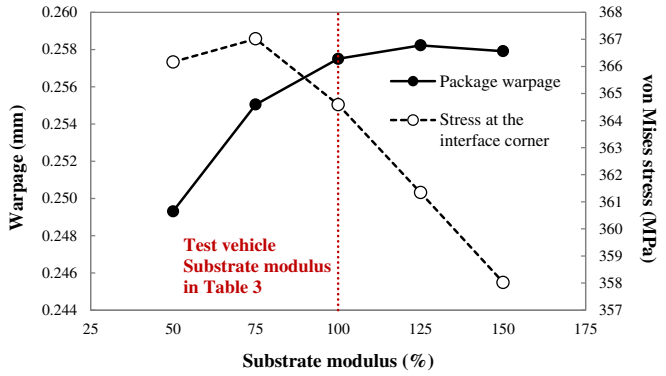


Fig. 13. Substrate modulus impact on package warpage and interface corner stress.

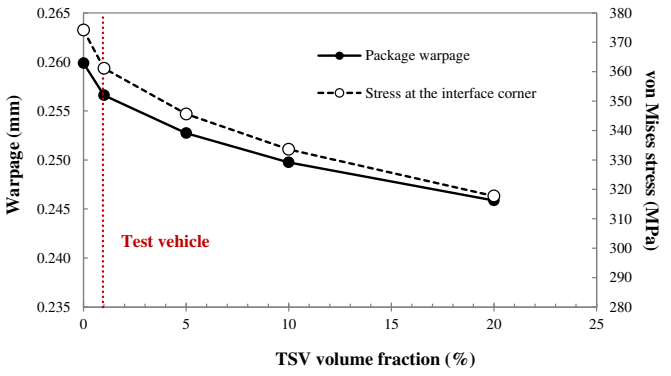


Fig. 15. TSV (Cu) volume fraction impact on package warpage and interface corner stress.

pared to chip and substrate due to its relatively low modulus and thin thickness. In addition, the stiffener makes the substrate more rigid. Thus, the influence of underfill on package warpage is not significant. Meanwhile, the interface corner stress at interposer is highly dependent on the underfill material. Low modulus, low CTE, and high T_g of the underfill can lower the stress.

Figs. 13 and 14 show the results of the substrate material property impact. For the substrate, T_g effect was not considered. It was found that a low modulus and low CTE of the substrate can prevent the warpage and stress development. Although Fig. 13 is presenting a low interface stress at a higher modulus substrate, the amount is not significant. As shown in Fig. 14, the warpage and stress vary dramatically by CTE change of the substrate. A low CTE substrate greatly decreases the warpage and stress.

Additional simulations were carried out to study the structural parameter effects. First, the effect of the TSV (Cu) volume fraction was investigated. The result with respect to the TSV volume fraction is shown in Fig. 15. The effective material property depending on the TSV volume fraction was calculated by Eq. (1) and (2) and assigned to the interposer material property. It can be seen that larger TSV volumes reduce the warpage of the package and stress at the interface. The interposer containing more TSVs acts like a buffer layer between the substrate and the ASIC since the CTE of Cu (16.5 ppm/°C) is similar to the substrate CTE. In Fig. 16, the effect of the substrate thickness is plotted. Thicker substrates lower the warpage and stress in the observed thickness range.

The optimization study indicates that employing a low CTE and a thick substrate is the most efficient way to reduce the package warpage. To minimize the interfacial stress, low modulus, low CTE, and high T_g for the underfill material is recommended. Current study focused on the package level optimization. Board level study is required to search the impact of suggested material properties and dimensions on solder joint reliability.

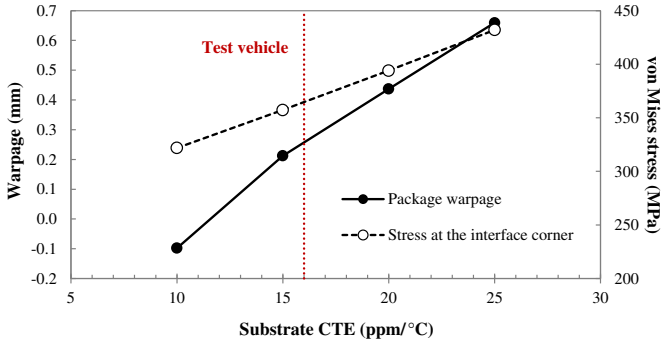


Fig. 14. Substrate CTE impact on package warpage and interface corner stress.

5. Conclusion

In this work, the out-of-plane displacement of the TSV interposer package was investigated during manufacturing process. Four kinds of samples were selected in the course of production to measure the warpage change during the assembly steps. DIC technique was employed to measure the real-time package warpage and the CTE of materials. DMA was executed to characterize the modulus of the substrate. In the numerical study, 3D FEA model was developed to predict the warpage. The C4/underfill layer, micro bump/underfill layer, and TSV interposer were treated as isotropic materials and the in-plane effective material properties were applied for simplicity. To obtain a more reliable simulation model, the simulation mimicked the actual assembly process. The simulation result in prior manufacturing steps was used for the analysis of the next assembly step. The validated FEA model was established by comparing it to the experimental result. In addition, parametric studies have been conducted by the verified simulation. It was demonstrated that a low modulus, low CTE, and high T_g for the underfill, and a low modulus and low CTE substrate can prevent the package warpage and stress development at the corner of interface between interposer and underfill. Additionally, an interposer with a higher Cu volume can decrease the warpage of the package and stress at the interface.

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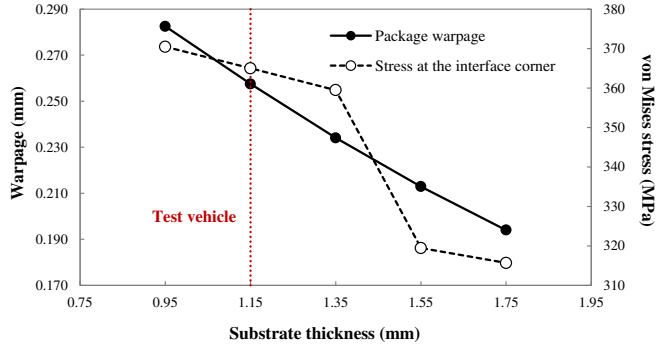

Fig. 16. Substrate thickness impact on package warpage and interface corner stress.

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